ACADEMIC REGULATIONS

COURSE STRUCTURE

AND

DETAILED SYLLABI

For

MASTER OF TECHNOLOGY

In

VLSI

(For the batches admitted from 2016-2017)

CHOICE BASED CREDIT SYSTEM

SREE VIDYANIKETHAN ENGINEERING COLLEGE

(AUTONOMOUS)

(Affiliated to JNTU Anantapur, Approved by AICTE
Programs Accredited by NBA; NAAC with 'A' grade)
Sree Sainath Nagar, A.Rangampet, Near Tirupati - 517 102.A.P.

VISION

To be one of the Nation's premier Engineering Colleges by achieving the highest order of excellence in Teaching and Research.

MISSION

- To foster intellectual curiosity, pursuit and dissemination of knowledge.
- To explore students' potential through academic freedom and integrity.
- To promote technical mastery and nurture skilled professionals to face competition in ever increasing complex world.

QUALITY POLICY

Sree Vidyanikethan Engineering College strives to establish a system of Quality Assurance to continuously address, monitor and evaluate the quality of education offered to students, thus promoting effective teaching processes for the benefit of students and making the College a Centre of Excellence for Engineering and Technological studies.

Department of Electronics and Communication Engineering

Vision

To be a center of excellence in Electronics and Communication Engineering through teaching and research producing high quality engineering professionals with values and ethics to meet local and global demands.

Mission

- The Department of Electronics and Communication Engineering is established with the cause of creating competent professionals to work in multicultural and multidisciplinary environments.

- Imparting knowledge through contemporary curriculum and striving for development of students with diverse background.

- Inspiring students and faculty members for innovative research through constant interaction with research organizations and industry to meet societal needs.

- Developing skills for enhancing employability of students through comprehensive training process.

- Imbibing ethics and values in students for effective engineering practice.

M. Tech. (VLSI)

Program Educational Objectives

After few years of graduation, the graduates of M. Tech. (VLSI) Program would have

PEO1. Enrolled or completed research studies in the core or allied areas of VLSI.

PEO2. Successful entrepreneurial or technical career in the core or allied areas of VLSI.

PEO3. Continued to learn and to adapt to the world of constantly evolving technologies in the core or allied areas of VLSI.

Program Outcomes

On successful completion of the Program, the graduates of M. Tech. (VLSI) Program will be able to

PO1. Demonstrate in-depth knowledge of specific discipline or professional area, including wider and global perspective, with an ability to discriminate, evaluate, analyze and synthesize existing and new knowledge, and integration of the same for enhancement of knowledge.

PO2. Analyze complex engineering problems critically, apply independent judgment for synthesizing information to make intellectual and/or creative advances for conducting research in a wider theoretical, practical and policy context.

PO3. Think laterally and originally, conceptualize and solve engineering problems, evaluate a wide range of potential solutions for those problems and arrive at feasible, optimal solutions after considering public health and safety, cultural, societal and environmental factors in the core areas of expertise.

PO4. Extract information pertinent to unfamiliar problems through literature survey and experiments, apply appropriate research methodologies, techniques and tools, design, conduct experiments, analyze and interpret data, demonstrate higher order skill and view things in a broader perspective, contribute individually/in group(s) to the development of scientific/technological knowledge in one or more domains of engineering.

PO5. Create, select, learn and apply appropriate techniques, resources, and modern engineering and IT tools, including prediction and modeling, to complex engineering activities with an understanding of the limitations.

PO6. Possess knowledge and understanding of group dynamics, recognize opportunities and contribute positively to collaborative-multidisciplinary scientific research, demonstrate a capacity for self-management and teamwork, decision-making based on open-mindedness, objectivity and rational analysis in order to achieve common goals and further the learning of themselves as well as others.

PO7. Demonstrate knowledge and understanding of engineering and management principles and apply the same to one's own work, as a member and leader in a team, manage projects efficiently in respective disciplines and multidisciplinary environments after consideration of

economical and financial factors.

PO8. Communicate with the engineering community, and with society at large, regarding complex engineering activities confidently and effectively, such as, being able to comprehend and write effective reports and design documentation by adhering to appropriate standards, make effective presentations, and give and receive clear instructions.

PO9: Recognize the need for, and have the preparation and ability to engage in life-long learning independently, with a high level of enthusiasm and commitment to improve knowledge and competence continuously.

PO10. Acquire professional and intellectual integrity, professional code of conduct, ethics of research and scholarship, consideration of the impact of research outcomes on professional practices and an understanding of responsibility to contribute to the community for sustainable development of society.

PO11. Observe and examine critically the outcomes of one's actions and make corrective measures subsequently, and learn from mistakes without depending on external feedback.

Programme Specific Outcomes

On successful completion of the Program, the graduates of M. Tech. (VLSI) Program will be able to

PSO1. Demonstrate in-depth knowledge of analog, digital and mixed signal integrated circuits with global perspective and an ability to process and integrate the existing and new knowledge for enhancement of knowledge.

PSO2. Analyze complex engineering problems critically and synthesize information to make intellectual and creative advances in the domains of analog, digital and mixed signal integrated circuits.

PSO3. Design and Develop solutions for real world problems in the domains of analog, digital and mixed signal integrated circuits.

PSO4. Provide a wide range of feasible and optimal solutions for complex engineering problems in the domains of analog, digital and mixed signal integrated circuits.

PSO5. Do research contributions individually or in groups to the development of scientific/ technological knowledge in the domains of analog, digital and mixed signal integrated circuits.

PSO6. Apply appropriate techniques, resources, and modern tools to complex engineering activities in the domains of analog, digital and mixed signal integrated circuits.

The Challenge of Change

"Mastery of change is in fact the challenge of moving human attention from an old state to a new state. Leaders can shift attention at the right time and to the right place. The real crisis of our times is the crisis of attention. Those who lead are the ones who can hold your attention and move it in a purposeful way. Transformation is nothing but a shift in attention from one form to another. The form of a beautiful butterfly breaks free from a crawling caterpillar. If you pay enough attention, you would be able to see how the butterfly hides within the caterpillar. The leader points out a butterfly when the follower sees only a caterpillar".

- Debashis Chatterjee

ACADEMIC REGULATIONS
CHOICE BASED CREDIT SYSTEM
M. Tech. Regular Two Year Degree Program
(for the batches admitted from the academic year 2016–17)

For pursuing Two year degree program of study in Master of Technology (M.Tech) offered by Sree Vidyanikethan Engineering College under Autonomous status and herein after referred to as SVEC (Autonomous):

1. Applicability : All the rules specified herein, approved by the Academic Council, shall be in force and applicable to students admitted from the academic year 2016-2017 onwards. Any reference to "College" in these rules and regulations stands for SVEC (Autonomous).

2. Extent: All the rules and regulations, specified hereinafter shall be read as a whole for the purpose of interpretation and as and when a doubt arises, the interpretation of the Chairman, Academic Council is final. It shall be ratified by Academic Council in the forth coming meeting. As per the requirements of statutory bodies, Principal, SVEC (Autonomous) shall be the Chairman, Academic Council.

3. Admission :

3.1. Admission into the Two Year M. Tech. Degree Program of study in Engineering:

3.1.1. Eligibility:

- A candidate seeking admission into the two year M. Tech Degree Program should have

  (i) Passed B.Tech / B.E or equivalent Program recognized by JNTUA, Anantapuramu, for admission as per the guidelines of Andhra Pradesh State Council of Higher Education (APSCHE).

  (ii) A minimum percentage of marks in the qualifying degree as prescribed by the AICTE / UGC or Government at the time of admission.

  (iii) Rank / score secured in the PGECET / GATE examination conducted by APSCHE/ MHRD for allotment of a seat by the convener PGECET, for admission.

3.1.2. Admission Procedure:

Admissions are made into the two year M.Tech. Degree Program as per the stipulations of APSCHE, Government of Andhra Pradesh:

(a) By the Convener, PGECET (for Category–A Seats)

(b) By the Management (for Category-B Seats).

4. Programs of study offered leading to the award of M.Tech. Degree and Eligibility:

Following are the two year postgraduate degree Programs of study offered in various branches at in SVEC (Autonomous) leading to the award of M.Tech. degree and eligibility to get admission into the Programs:

Name of the specialization	Offered by the Department	Name of the Degree / Branch eligible for Admission
Electrical Power Systems	EEE	BE/ B.Tech / AMIE in Electrical & Electronics Engineering / Electrical Engineering or equivalent
Digital Electronics and Communication Systems	ECE	BE / B.Tech in ECE / AMIE in ECE, AMIE (Electronics & Telecommunication Engineering) / AMIETE (Electronics & Telematics Engineering)/ Electronics & Computer Engineering/ Electronics/ Electronics & Telematics or equivalent
Communication Systems		
VLSI		BE / B.Tech / AMIE in ECE, / EEE / CSE / Electronics & Computer Engineering / ETE / IT / CSIT / Electronics and Control Engineering / Instrumentation Engineering / Instrumentation Technology / EIE / Electronics Engineering / Bio-Medical Engineering / AMIETE (Electronics & Telematics Engineering)/ Electronics or equivalent
Computer Science	CSE	BE / B.Tech / AMIE in CSE / CSIT / IT / CSSE , M. Sc. (Computer Science), M. Sc. (Information Systems), M. Sc. (Information Technology), MCA or equivalent.
Computer Networks and Information Security		
Software Engineering	IT	

5. Duration of the Program:

5.1 Minimum Duration: The program will extend over a period of two years leading to the Degree of Master of Technology (M.Tech) of the JNTUA, Ananthapuramu. The two academic years will be divided into four semesters with two semesters per year. In first year, each semester shall normally consist of 22 weeks (≥90 working days) having – 'Continuous Internal Evaluation (CIE)' and 'Semester End Examination (SEE)'. In second year, each semester shall consists of 18 weeks and the entire year is for project work. Choice Based Credit System (CBCS) and Credit Based Semester System (CBSS) as suggested by UGC, and Curriculum/ Course Structure as suggested by AICTE are followed.

5.2 Maximum Duration: The student shall complete all the passing requirements of the M.Tech degree program within a maximum duration of 4 years including Gap year, this duration reckoned from the commencement of the semester to which the student was first admitted to the program.

I SEMESTER (22 weeks)	**INSTRUCTION PERIOD**:	I Spell : 7 Weeks II Spell : 9 Weeks	16 Weeks
	Internal Examinations :	I Mid : 1 week II Mid : 1 week	2 Weeks
	Preparation & Practical Examinations		2 Week
	External Examinations		2 Weeks
	Semester Break		2 Weeks
II SEMESTER (22 weeks)	**INSTRUCTION PERIOD**:	I Spell : 7 Weeks II Spell : 9 Weeks	16 weeks
	Internal Examinations :	I Mid : 1 week II Mid : 1 week	2 Weeks
	Preparation & Practical Examinations		2 Week
	External Examinations		2 Weeks
	Summer Vacation		4 Weeks
III SEMESTER	Project Work Phase – I		19 Weeks
IV SEMESTER	Project Work Phase – II		19 Weeks
	Project Work Viva-Voce examinations		2 Weeks

6. Course Structure: Each Program of study shall consist of:

- Professional core courses:

  The list of professional core courses are chosen as per the suggestions of the experts, to impart knowledge and skills needed in the concerned specialization of study.

- Professional elective courses:

  Professional elective courses shall be offered to the students to diversify their spectrum of knowledge and skills. The elective courses can be chosen based on the interest of the student to broaden his individual knowledge and skills.

- Audit Courses: Audit courses shall be offered to the students to diversify their knowledge.

Contact periods: Depending on the complexity and volume of the course the number of contact periods per week shall be assigned.

7. Credit System: All Courses are to be registered by a student in a Semester to earn Credits. Credits are assigned based on the following norms given in Table 1.

Table 1

Course	Periods/Week	Credits
Theory	01	01
Practical	04	02
Seminar	--	02
Project Work Phase-I	--	--
Project Work Phase-II	--	28

i. As a norm, for the theory courses, **one credit** for one contact period per week is assigned.

ii. As a norm, for practical courses **two credits** will be assigned for four contact periods per week.

iii. For courses like Project/Seminar, where formal contact periods are not specified, credits are assigned based on the complexity of the work to be carried out.

iv. There are no credits for audit courses.

Other student activities like NCC, NSS, Sports, Study Tour, Guest Lecture etc. will not carry Credits.

The two year curriculum of any M. Tech Degree Program of study shall have total of **86** credits (28 credits in I Semester, 30 credits in II Semester and 28 credits in IV Semester).

8. Choice Based Credit System (CBCS):

Choice Based Credit System (CBCS) is introduced based on UGC guidelines in order to promote:

- Student centered learning
- Cafeteria approach
- Students to learn courses of their choice
- Learning at their own pace
- Interdisciplinary learning

- A student is introduced to "Choice Based Credit System (CBCS)"
- The total credits for the Programme is 86.
- A student has choice of registering for credits from the theory courses offered in the program ensuring the total credits in a semester are between 24 and 34.
- In I Semester, the student has the option of registering for one additional theory course from the latter semester or dropping one existing theory course from the current semester within the course structure of the program. In II Semester also, the student has the option of registering for one additional theory course from the previous semester if dropped earlier within the course structure of the program. However the maximum number of credits the student can register in a particular semester cannot exceed 33 credits.
- Grade points, based on percentage of marks awarded for each course will form the basis for calculation of SGPA (Semester Grade Point Average) and CGPA (Cumulative Grade Point Average).
- All the registered credits will be considered for the calculation of final CGPA.

9. Course Enrollment and Registration

9.1 Each student, on admission shall be assigned to a Faculty Advisor (Mentor) who shall advice and counsel the student about the details of the academic programme and the choice of courses considering the student's academic background and career objectives.

9.2 The enrollment of courses in I Semester will commence on the day of admission. If the student wishes, the student may drop or add courses (vide clause 8) within **three** days before commencement of I semester class work and complete the registration process. The student shall enroll for the courses with the help of the student's Faculty Advisor (Mentor). The enrollment of courses in II Semester will commence 10 days prior to the last instructional day of the I semester and complete the registration process for all the remaining theory courses as per program course structure, duly authorized by the Chairman, Board of studies of concern department.

9.3 If any student fails to register the courses in a semester, he shall undergo the courses as per the program structure.

9.4 After registering for a course, a student shall attend the classes, satisfy the attendance requirements, earn Continuous Assessment marks and appear for the Semester-end Examinations.

9.5 No elective course shall be offered by a Department unless a minimum of 8 students register for the course.

10. Massive Open Online Course (MOOC)

A Massive Open Online Course (MOOC) is an online course aimed at unlimited participation and open access via the web. MOOC is a model for delivering learning content online to any person who takes a course, with no limit on attendance.

- A student shall undergo a "Massive Open Online Course (MOOC)" for award of the degree besides other requirements.
- A student is offered this Online Course at the beginning of his II Semester of study and the course has to be completed by the end of III Semester. If the student fails to complete the course by the end of III Semester, it shall be treated as a backlog and needs to be completed before completion of the program for the award of the degree.
- The student shall confirm registration by enrolling the course within 10 days prior to the last instructional day of the I semester like other courses.
- The courses will be approved by the Chairman, Academic Council, SVEC based on the recommendations of the Chairman, Board of Studies of concerned program considering current needs.
- A student has a choice of registering for only one MOOC with the recommendation of Chairman, Board of studies of concerned program and duly approved by the Chairman, Academic Council, SVEC.
- The student shall undergo MOOC without disturbing the normal schedule of regular class work.
- One faculty member assigned by the Head of the Department shall be responsible for the periodic monitoring of the course implementation.
- No formal lectures need be delivered by the faculty member assigned to the students.
- If any student wants to change the MOOC course already registered, he will be given choice to register a new MOOC course in M. Tech. II / III Semester only, with the recommendation of Chairman, Board of studies of concerned program and duly approved by the Chairman, Academic Council, SVEC.
- Finally, the performance of the student in the course will be evaluated as stipulated by the course provider. A certificate will be issued on successful completion of the course by the course provider.
- The performance in the MOOC will not be considered for the calculation of SGPA and CGPA of the student.
- The MOOC course will be listed in the grade sheets of the student.

11. Break of Study from a Programme (Gap Year)

11.1 A student is permitted to go on break of study for a maximum period of one year.

11.2 The student shall apply for break of study in advance, in any case, not later than the last date of the first assessment period in a semester. The application downloaded from website and duly filled by the student shall be submitted to the Head of the Department. In the case of start-up for incubation of idea only, the application for break of study shall be forwarded by the Head of the Department

to the Principal, SVEC. A sub-committee appointed by the principal shall give recommendations for approval.

11.3 The students permitted to rejoin the programme after break of study shall be governed by the Curriculum and Regulations in force at the time of rejoining. The students rejoining in new regulations shall apply to the Principal, SVEC in the prescribed format through Head of the Department at the beginning of the readmitted semester itself for prescribing additional/equivalent courses, if any, from any semester of the regulations in-force, so as to bridge the curriculum in-force and the old curriculum.

11.4 The total period for completion of the programme reckoned from the commencement of the I Semester to which the student was admitted shall not exceed the maximum period specified in clause 5.2 irrespective of the period of break of study in order that the student may be eligible for the award of the degree (vide clause 19).

11.5 If a student has not reported to the department after approved period of break of study without any intimation, the student is treated as detained in that semester. Such students are eligible for readmission for the semester when offered next.

12. Examination System: All components in any Program of study shall be evaluated through internal evaluation and / or an external evaluation conducted as semester-end examination.

12.1. Distribution of Marks:

<table>
<tr><th>Sl. No.</th><th>Course</th><th>Marks</th><th>Examination and Evaluation</th><th>Scheme of examination</th></tr>
<tr><td rowspan="3">1.</td><td rowspan="3">Theory</td><td>60</td><td>Semester-end examination of 3 hours duration (External evaluation)</td><td>The examination question paper in theory courses shall be for a maximum of 60 marks. The question paper shall be of descriptive type with 5 questions, taken one from each unit of syllabus, having internal choice and all 5 questions shall be answered. All questions carry equal marks.</td></tr>
<tr><td rowspan="2">40</td><td rowspan="2">Mid-term Examination of 2 hours duration (Internal evaluation).</td><td>The question paper shall be of descriptive type with 5 essay type questions out of which 4 are to be answered and evaluated for 40 marks.</td></tr>
<tr><td>Two mid-term examinations each for 40 marks are to be conducted. For a total of 40 marks, 75% of better one of the two and 25% of the other one are added and finalized.
Mid-I: After first spell of instruction (I to II Units).
Mid-II: After second spell of instruction (III to V Units).</td></tr>
</table>

Sl. No.	Course	Marks	Examination and Evaluation		Scheme of examination
2	Laboratory	50	Semester-end Lab Examination for 3 hours duration (External evaluation)		50 marks are allotted for laboratory examination during semester-end.
		50	30	Day-to-Day evaluation for Performance in laboratory experiments and Record. (Internal evaluation).	Two laboratory examinations, which includes Day-to-Day evaluation and Practical test, each for 50 marks are to be evaluated. For a total of 50 marks 75% of better one of the two and 25% of the other one are added and finalized. **Laboratory examination-I:** Shall be conducted just before I mid-term examinations. **Laboratory examination-II:** Shall be conducted just before II mid-term examinations.
			20	Practical test (Internal evaluation).	
3	Audit Course	-	-		Audit course will be conducted as given in 12.2.1
4	Seminar	100	Semester-end Examination		100 marks are allotted for Seminar during semester-end evaluation by the Departmental Committee (DC) as given in 12.2.2.
5	Project Work	400	200	External evaluation	Semester-end Project Viva-Voce Examination by Committee as detailed in 12.2.3.
			200	Internal evaluation	Continuous evaluation by the DC as detailed in 12.2.3.

12.2 Audit Course/ Seminar/Project Work Evaluation:

12.2.1. Audit Course: For audit course, attendance shall be maintained like in case of any regular course. Students may be encouraged to submit assignments and give presentations on the course topics. There won't be any examinations for audit courses. However, the courses shall be listed in the grade sheet of the student.

12.2.2. Seminar: For the seminar, the student shall collect information through literature survey on a specialized topic and prepare a technical report, showing his understanding over the topic, and submit to the Department a week before presentation. The report and the presentation shall be evaluated at the end of the semester during the period of preparation and practicals by the Departmental Committee (DC) consisting of two senior faculty members and concerned supervisor of the department. The DC is constituted by the Principal on the recommendations of the Head of the Department. The department shall have individual DCs for each M. Tech. Program with senior faculty members and the supervisor specialized in the program.

12.2.3. Project Work:

12.2.3.1. Student shall register for the Project work with the approval of DC in the III Semester and continue the work in the IV Semester too. The DC shall monitor the progress of the project work. In III Semester, Phase–I

of the Project Work has to be completed. A Student has to identify the topic of work, collect relevant Literature, preliminary data, implementation tools/ methodologies etc., and perform a critical study and analysis of the problem identified. He shall submit status report in two different phases in addition to oral presentation before the DC for evaluation and award of internal marks at the end of Phase –I. A candidate shall continue the Project Work in IV Semester (Phase – II) and submit a Project report at the end of Phase–II after approval of the DC. During Phase–II, the student shall submit status report in two different phases, in addition to oral presentation before the DC. The DC shall evaluate the project based on the progress, presentations and quality of work. A candidate shall be allowed to submit the dissertation only after passing all the courses from 1st to 3rd semesters and on recommendations of the DC. The Viva-Voce examination shall be conducted as per the IV Semester examinations schedule.

12.2.3.2 Three copies of the dissertation certified in the prescribed form by the concerned Supervisor and HOD shall be submitted to the Department. One copy is to be submitted to the Chief Controller of Examinations, SVEC (Autonomous) and one copy to be sent to the examiner. The examiner shall be nominated by the Chief Controller of the Examinations from the panel of three examiners submitted by the Department for a maximum of 5 students at a time for adjudication.

12.2.3.3 If the report of the examiner is favorable, Viva-Voce examination shall be conducted by a board consisting of the concerned Supervisor, Head of the Department and the examiner who adjudicated the dissertation. The board shall jointly evaluate the candidates project work. If the report of the examiner is not favorable, the candidate should revise and resubmit the project report followed by Viva-Voce examination.

12.2.3.4 The candidates who fail in Viva-Voce examination shall have to re-appear the Viva-Voce examination after three months. Extension of time within the total permissible limit for completing the project is to be obtained from the Chairman, Academic Council, SVEC (Autonomous).

12.2.3.5 If a candidate desires to change the topic of the project already chosen, during Phase–II, he has to re-register for Project work with the approval of the DC and repeat Phases–I & II. Marks already earned in Phase–I stand cancelled.

12.2.3.6 If a candidate unable to complete the project work after Phase–II and desires to change the topic of the project already chosen, he has to re-register for Project work with the approval of the DC and repeat Phases–I & II. Marks already earned in Phase–I & II stand cancelled.

12.3. Eligibility to appear for the semester-end examination:

12.3.1 A student shall be eligible to appear for semester-end examinations if he acquires a minimum of 75% of attendance in aggregate of all the courses in a semester.

12.3.2 Condonation of shortage of attendance in aggregate up to 10% (65% and above and below 75%) in each semester may be granted by the College Academic Committee.

12.3.3 Shortage of attendance below 65% in aggregate shall in no case be condoned.

12.3.4 Students whose shortage of attendance is not condoned in any semester shall not be eligible to take their semester-end examination and their registration shall stand cancelled.

12.3.5 A student shall not be promoted to the next semester unless he satisfies the attendance requirements of the semester, as applicable. The student may seek readmission for the semester when offered next. He will not be allowed to register for the courses of the semester while he is in detention.

12.3.6 A stipulated fee shall be payable to the college towards condonation of shortage of attendance.

12.4. Evaluation: Following procedure governs the evaluation.

12.4.1. Marks for components evaluated internally by the faculty should be submitted to the Controller of Examinations one week before the commencement of the semester-end examinations. The marks for the internal evaluation components shall be added to the external evaluation marks secured in the semester-end examinations, to arrive at total marks for any course in that semester.

12.4.2. Performance in all the courses is tabulated course-wise and shall be scrutinized by the Results Committee and moderation is applied if needed, and course-wise marks are finalized. Total marks obtained in each course are converted into letter grades.

12.4.3. Student-wise tabulation shall be done and individual grade sheet shall be generated and issued.

12.5. Personal verification / Revaluation / Recounting:

Students shall be permitted for personal verification/request for recounting/ revaluation of the semester-end examination answer scripts within a stipulated period after payment of prescribed fee. After recounting or revaluation, records shall be updated with changes if any and the student shall be issued a revised grade sheet. If there are no changes, the student shall be intimated the same through a notice.

12.6. Supplementary Examination:

In addition to the regular semester-end examinations conducted, the College may also schedule and conduct supplementary examinations for all the courses of other semesters when feasible for the benefit of students. Such of the candidates writing supplementary examinations may have to write more than one examination per day.

13. Re-Registration for Improvement of Internal Marks:

Following are the conditions to avail the benefit of improvement of internal evaluation marks.

13.1 The candidate should have completed the course work and obtained examinations results for I and II semesters.

13.2 Out of the courses the candidate has failed in the examinations due to internal evaluation marks secured being less than 50%, the candidate shall be given one chance for a maximum of 3 theory courses for improvement of internal evaluation marks.

13.3 He should have passed all the remaining courses for which the internal evaluation marks secured more than or equal to 50%.

13.4 The candidate has to register for the chosen courses and fulfill the academic requirements.

13.5 For each course, the candidate has to pay a fee equivalent to one third of the semester tuition fee and the amount is to be remitted in the form of D.D./ Challan in favour of the Principal, Sree Vidyanikethan Engineering College payable at Tirupati along with the requisition through the concerned Head of the Department.

13.6 In the event of availing the Improvement of Internal evaluation marks, the internal evaluation marks as well as the semester-end examinations markssecured in the previous attempt(s) for the re-registered courses stand cancelled.

14. Academic Requirements for completion of M.Tech Program of study:

The following academic requirements have to be satisfied in addition to the attendance requirements for completion of M.Tech Program of study.

14.1 A student shall be deemed to have satisfied the minimum academic requirements for each theory, laboratory and project work, if he secures not less than 40% of marks in the semester-end examination and a minimum of 50% of marks in the sum total of the internal evaluation and semester-end examination taken together. For the seminar, he should secure not less than 50% of marks in the semester-end examination.

14.2 A student shall register for all the 86 credits and earn all the 86 credits. Marks obtained in the 86 credits shall be considered for the calculation of the DIVISION based on CGPA.

14.3 A student who fails to earn 86 credits as indicated in the curriculum within **four** academic years from the year of his admission shall forfeit his seat in M.Tech. Program and his admission stands cancelled.

15. Transitory Regulations:

Students who got detained for want of attendance (**or**) who have not fulfilled academic requirements (**or**) who have failed after having undergone the Program in earlier regulations (**or**) who have discontinued and wish to continue the Program are eligible for admission into the unfinished semester from the date of commencement of class work with the same (**or**) equivalent courses as and when courses are offered and they will be in the academic regulations into which they are presently readmitted.

A regular student has to satisfy all the eligibility requirements within the maximum stipulated period of **four years** for the award of M.Tech Degree.

16. Grades, Grade Point Average and Cumulative Grade Point Average:

16.1. Grade System: After all the components and sub-components of any course (including laboratory courses) are evaluated, the final total marks obtained shall be converted to letter grades on a "**10 point scale**" as described below.

Grades conversion and Grade points allotted

% of Marks obtained	Grade	Description of Grade	Grade Points (GP)
≥ 95	O	Outstanding	10
≥ 85 to < 95	S	Superior	9
≥ 75 to < 85	A	Excellent	8
≥ 65 to < 75	B	Very Good	7
≥ 55 to < 65	C	Good	6
≥ 50 to <55	D	Pass	5
< 50	F	Fail	0
Not Appeared	N	Absent	0

Pass Marks: A student shall be declared to have passed theory course, laboratory course and project work if he secures minimum of 40% marks in Semester-end examination, and a minimum of 50% marks in the sum total of internal evaluation and Semester-end examination taken together. For the seminar, he shall be declared to have passed if he secures minimum of 50% of marks in the semester-end examinations. Otherwise he shall be awarded fail grade - **F** in such a course irrespective of internal marks. **F** is considered as a fail grade indicating that the student has to pass the semester-end examination in that course in future and obtain a grade other than **F** and **N** for passing the course.

16.2. Semester Grade Point Average (SGPA):

Semester Grade Point Average (SGPA) shall be calculated as given below on a "10 point scale" as an index of the student's performance at the end of each semester:

$$\text{SGPA} = \frac{\sum(C\ X\ GP)}{\sum C}$$

where ***C*** denotes the credits assigned to the courses undertaken in that semester and ***GP*** denotes the grade points earned by the student in the respective courses.

Note: *SGPA is calculated only for the candidates who passed all the courses in that semester.*

16.3. Cumulative Grade Point Average (CGPA):

The CGPA for any student is awarded only when he completes the Program i.e., when the student passes in all the courses prescribed in the Program. The CGPA is computed on a 10 point scale as given below:

$$\text{CGPA} = \frac{\sum(C\ X\ GP)}{\sum C}$$

where ***C*** denotes the credits assigned to courses undertaken up to the end of the Program and *GP* denotes the grade points earned by the student in the respective courses.

17. Grade Sheet: A grade sheet (Marks Memorandum) shall be issued to each student indicating his performance in all courses registered in that semester indicating the SGPA.

18. Transcripts: After successful completion of the entire Program of study, a transcript containing performance in all academic years shall be issued as a final record. Duplicate transcripts will also be issued, if required, after payment of requisite fee. Partial transcript will also be issued upto any point of study to a student on request.

19. Award of Degree: The Degree shall be conferred and awarded by Jawaharlal Nehru Technological University Anantapur, Ananthapuramu on the recommendations of the Chairman, Academic Council, SVEC (Autonomous).

19.1. Eligibility: A student shall be eligible for the award of M.Tech Degree if he fulfills all the following conditions:

- Registered and successfully completed all the components prescribed in the Program of study to which he is admitted.
- Successfully acquired the minimum required credits as specified in the curriculum corresponding to the Program of study within the stipulated time.
- Obtained CGPA greater than or equal to 5.0 (Minimum requirement for declaring as passed).
- Has no dues to the College, Hostel, Library etc. and to any other amenities provided by the College.
- No disciplinary action is pending against him.

19.2. Award of Division: Declaration of division is based on CGPA.

Awarding of Division

CGPA	Division
> = 7.0	First Class with Distinction
> = 6.0 and < 7.0	First Class
> = 5.0 and < 6.0	Second Class

20. Additional academic regulations:

20.1 A student may appear for any number of supplementary examinations within the stipulated time to fulfill regulatory requirements for award of the degree.

20.2 In case of malpractice/improper conduct during the examinations, guidelines shall be followed as shown in the **Annexure-I**.

20.3 When a student is absent for any examination (Mid-term or Semester-end) he shall be awarded **zero** marks in that component (course) and grading will be done accordingly.

20.4 When a component is cancelled as a penalty, he shall be awarded zero marks in that component.

21. Withholding of Results:

If the candidate has not paid dues to the College/University (or) if any case of indiscipline is pending against him, the result of the candidate shall be withheld and he will not be allowed/promoted to the next higher semester

22. Amendments to regulations:

The Academic Council of SVEC (Autonomous) reserves the right to revise, amend, or change the Regulations, Scheme of Examinations, and / or Syllabi or any other policy relevant to the needs of the society or industrial requirements etc., with the recommendations of the concerned Board(s) of Studies.

23. General:

The words such as "he", "him", "his" and "himself" shall be understood to include all students irrespective of gender connotation.

Note: *Failure to read and understand the regulations is not an excuse.*

Annexure-I

GUIDE LINES FOR DISCIPLINARY ACTION FOR MALPRACTICES / IMPROPER CONDUCT IN EXAMINATIONS

Rule No.	Nature of Malpractices/ Improper conduct	Punishment
	If the candidate:	
1. (a)	Possesses or keeps accessible in examination hall, any paper, note book, programmable calculators, Cell phones, pager, palm computers or any other form of material concerned with or related to the course of the examination (theory or practical) in which he is appearing but has not made use of (material shall include any marks on the body of the candidate which can be used as an aid in the course of the examination)	Expulsion from the examination hall and cancellation of the performance in that course only.
(b)	Gives assistance or guidance or receives it from any other candidate orally or by any other body language methods or communicates through cell phones with any candidate or persons in or outside the exam hall in respect of any matter.	Expulsion from the examination hall and cancellation of the performance in that course only of all the candidates involved. In case of an outsider, he will be handed over to the police and a case is registered against him.
2.	Has copied in the examination hall from any paper, book, programmable calculators, palm computers or any other form of material relevant to the course of the examination (theory or practical) in which the candidate is appearing.	Expulsion from the examination hall and cancellation of the performance in that course and all other courses the candidate has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the courses of that Semester. The Hall Ticket of the candidate is to be cancelled.
3.	Impersonates any other candidate in connection with the examination.	The candidate who has impersonated shall be expelled from examination hall. The candidate is also debarred for four consecutive semesters from class work and all Semester-end examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat. The performance of the original candidate who has been impersonated, shall be cancelled in all the courses of the examination (including labs and project work) already appeared and shall not be allowed to appear for examinations of the remaining courses of that semester. The candidate is also debarred for four consecutive semesters from class work and all Semester-end examinations, if his involvement is established. Otherwise, The candidate is debarred for two consecutive semesters from class work and all Semester-end examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat. If the imposter is an outsider, he will be handed over to the police and a case is registered against him.
4.	Smuggles in the Answer book or additional sheet or takes out or arranges to send out the question paper during the examination or answer book or additional sheet, during or after the examination.	Expulsion from the examination hall and cancellation of performance in that course and all the other courses the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the courses of that semester. The candidate is also debarred for two consecutive semesters from class work and all Semester-end examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
5.	Uses objectionable, abusive or offensive language in the answer paper or in letters to the examiners or writes to the examiner requesting him to award pass marks.	Cancellation of the performance in that course only.
6.	Refuses to obey the orders of the Chief Controller of Examinations/Controller of Examinations/any officer on duty or misbehaves or creates disturbance of any kind in and around	In case of students of the college, they shall be expelled from examination halls and cancellation of their performance in that course and all other courses the candidate(s) has (have) already

	the examination hall or organizes a walk out or instigates others to walk out, or threatens the Controller of Examinations or any person on duty in or outside the examination hall of any injury to his person or to any of his relations whether by words, either spoken or written or by signs or by visible representation, assaults the Controller of Examinations, or any person on duty in or outside the examination hall or any of his relations, or indulges in any other act of misconduct or mischief which result in damage to or destruction of property in the examination hall or any part of the College campus or engages in any other act which in the opinion of the officer on duty amounts to use of unfair means or misconduct or has the tendency to disrupt the orderly conduct of the examination.	appeared and shall not be permitted to appear for the remaining examinations of the courses of that semester. If the candidate physically assaults the invigilator/Controller of the Examinations, then the candidate is also debarred and forfeits his/her seat. In case of outsiders, they will be handed over to the police and a police case is registered against them.
7.	Leaves the exam hall taking away answer script or intentionally tears of the script or any part thereof inside or outside the examination hall.	Expulsion from the examination hall and cancellation of performance in that course and all the other courses the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the courses of that semester. The candidate is also debarred for two consecutive semesters from class work and all Semester-end examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
8.	Possess any lethal weapon or firearm in the examination hall.	Expulsion from the examination hall and cancellation of the performance in that course and all other courses the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the courses of that semester. The candidate is also debarred and forfeits the seat.

Note: Whenever the performance of a student is cancelled in any course(s) due to Malpractice, he has to register for Semester-end Examinations in that course(s) consequently and has to fulfill all the norms required for the award of Degree.

SREE VIDYANIKETHAN ENGINEERING COLLEGE (Autonomous)

Sree Sainath Nagar, Tirupati – 517 102.

SVEC16 M. Tech. VLSI
Course Structure

I-Semester

S. No.	Course Code	Course Title	Contact Periods per Week				Credits	Scheme of Examination Max. Marks		
			L	T	P	Total		Internal Marks	External Marks	Total Marks
1.	16MT15701	Analog IC Design	4	-	-	4	4	40	60	100
2.	16MT15702	Computational Methods in Microelectronics	4	-	-	4	4	40	60	100
3.	16MT15703	Device Modeling	4	-	-	4	4	40	60	100
4.	16MT15704	Digital IC Design	4	-	-	4	4	40	60	100
5.	16MT15705	IC Fabrication	4	-	-	4	4	40	60	100
6.	***Professional Elective-1***		4	-	-	4	4	40	60	100
	16MT23808	Real Time Systems								
	16MT15706	Advanced Digital Signal Processing								
	16MT15707	FPGA Architectures and Applications								
	16MT15708	RFIC Design								
7.	16MT15731	Analog IC Design Lab	-	-	4	4	2	50	50	100
8.	16MT15732	Digital IC Design Lab	-	-	4	4	2	50	50	100
Total:			**24**	**-**	**8**	**32**	**28**	**340**	**460**	**800**
9.	16MT13808	Research Methodology (Audit Course)	-	2	-	2	-	-	-	-

II-Semester

S. No.	Course Code	Course Title	Contact Periods per Week				Credits	Scheme of Examination Max. Marks		
			L	T	P	Total		Internal Marks	External Marks	Total Marks
1.	16MT25701	Low Power VLSI Design	4	-	-	4	4	40	60	100
2.	16MT25702	Mixed Signal Design	4	-	-	4	4	40	60	100
3.	16MT25703	Nanoelectronics	4	-	-	4	4	40	60	100
4.	16MT25704	Physical Design Automation	4	-	-	4	4	40	60	100
5.	16MT25705	Testing and Testability	4	-	-	4	4	40	60	100
6.	***Professional Elective-2***		4	-	-	4	4	40	60	100
	16MT13806	ASIC Design								
	16MT25707	Co-Design								
	16MT25708	System-on-Chip Design and Verification								
	16MT25709	Wireless Sensor Networks								
7.	16MT25731	Mixed Signal and Physical Design Automation Lab	-	-	4	4	2	50	50	100
8.	16MT25732	Nanoelectronics Lab	-	-	4	4	2	50	50	100
9.	16MT25733	Seminar	-	-	-	-	2	--	100	100
Total:			**24**	**-**	**8**	**32**	**30**	**340**	**560**	**900**
10.	16MT23810	Intellectual Property Rights (Audit Course)	-	2	-	2	-	-	-	-

III-Semester

S. No.	Course Code	Course Title	Contact Periods per Week				Credits	Scheme of Examination Max. Marks		
			L	T	P*	Total		Internal Marks	External Marks	Total Marks
1.	16MT3MOOC	MOOC	-	-	-	-	-	-	-	-
2.	16MT35731	Project Work – Phase I	-	-	-	-	-	100	--	100
Total:			**-**	**-**	**-**	**-**	**-**	**100**	**--**	**100**

*Fulltime Project Work

IV-Semester

S. No.	Course Code	Course Title	Contact Periods per Week				Credits	Scheme of Examination Max. Marks		
			L	T	P*	Total		Internal Marks	External Marks	Total Marks
1.	16MT45731	Project Work – Phase II	-	-	-	-	28	100	200	300
Total:			**-**	**-**	**-**	**-**	**28**	**100**	**200**	**300**
Grand Total:							**86**	**880**	**1220**	**2100**

*Fulltime Project Work

M. Tech. - I SEMESTER
(16MT15701) ANALOG IC DESIGN

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	4	-	-	4

PREREQUISITE:

Courses on Semiconductor Devices and Circuits and VLSI design at UG Level.

COURSE DESCRIPTION:

MOS Device physics; Characteristics of amplifiers; Feedback circuits and operational amplifiers; Stability and frequency compensation of operational amplifiers; Nonlinear Analog circuits & other applications

COURSE OUTCOMES:
After successful completion of the course, students will be able to:
1. Demonstrate in-depth knowledge in
   - Sub threshold and Short Channel effects.
   - Current Mirrors.
   - Frequency response and Noise Characteristics of Amplifier.
   - Effect of Loading in Feedback Circuits.
   - One stage operational Amplifiers.
   - Ring Oscillator.
2. Analyze complex engineering problems critically in the domain of analog IC design for conducting research.
3. Design analog integrated Circuits for societal needs.
4. Develop Skills to solve engineering problems for feasible and optimal solutions in the core area of analog ICs.
5. Initiate research work on Reusable Design for the development of analog IC design.
6. Apply appropriate technique to implement accurate models for devices.

Detailed Syllabus:

Unit-I: Basic MOS Device Physics and Single Stage Amplifiers (Periods: 15)
Basic MOS Device Physics: General Considerations, MOS I/V Characteristics, Second-Order Effects.
Single Stage Amplifiers: Basic Concepts, Common-Source Stage, Source follower, Common Gate Stage, Cascode Stage, Differential Amplifiers-Single Ended and Differential Operation, Basic Differential Pair. Passive and Active Current Mirrors.

Unit-II: Frequency Response and Noise Characteristics of Amplifiers (Periods: 08)
Frequency Response-General Considerations, Common-Source Stage, Source follower, Common Gate Stage, Cascode Stage, Differential pair.
Noise-Statistical Characteristics of Noise, Noise in Single Stage Amplifiers, Noise in Differential Pairs.

Unit-III: Feedback Circuits and Operational Amplifiers (Periods: 12)
Feedback Circuits - General considerations, Feedback Topologies, Effect of Loading, Effect of Feedback on Noise.
Operational Amplifiers - General considerations, One-stage Op Amps, Two - stage Op Amps, Gain Boosting, Input range limitations, slew rate, power supply rejection, Noise in Op Amps.

Unit-IV: Stability & Frequency Compensation and Bandgap References
(Periods:10)

Stability & Frequency Compensation: General considerations, Multi pole Systems, Phase Margin, Frequency Compensation, Compensation of Two-Stage Op Amps.
Bandgap References: Supply-Independent Biasing, Temperature-independent References, PTAT Current Generation, Constant - Gm Biasing, Speed and Noise Issues.

Unit-V: Nonlinear Analog circuits & other applications (Periods: 10)
Sampling Switches, Switched-Capacitor Amplifiers, Switched capacitor integrator, Ring oscillators, Simple PLL.

Total Periods: 55

TEXT BOOK:

1. Behzad Razavi, "Design of Analog CMOS Integrated Circuit", Tata McGraw-Hill, 14th Reprint 2008.

REFERENCE BOOKS:

1. D.A. John & Ken Martin, "Analog Integrated Circuit Design", John Wiley & Sons, 1997.
2. Philip Allen & Douglas Holberg, "CMOS Analog Circuit Design", Oxford University Press, 2002.

M. Tech. - I Semester
(16MT15702) COMPUTATIONAL METHODS IN MICROELECTRONICS

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	4	-	-	4

PRE-REQUISITES:
A Course on Mathematics at UG Level.

COURSE DESCRIPTION:
Linear and Nonlinear Systems modeling; Approximation; Interpolation; Curve Fitting; Numerical Integration; Finite Difference Techniques; Initial Value problems; Energy Methods and Minimization; Finite Element Methods; Dynamic methods; Method of Characteristics; Finite Volume Methods; Grid Generation and Error Estimation; Device and Process Simulation; Layout and Yield estimation algorithms; Symbolic analysis and Synthesis of Analog ICs.

COURSE OUTCOMES:
After successful completion of the course, students will be able to:
1. Gain in-depth knowledge in
   - Computation Tools.
   - FDM, FEM, FVM.
   - Grid Generation.
   - Refinement Algorithms.
   - Errors in Meshing.
   - Application to device and process simulation.
2. Analyze the errors of Computational tools and judge independently the best suited Tool for fast Computation of simulation for conducting research in CAD Tools design.
3. Develop skills to solve problems of Meshing, Grid Generation to improve speed and accuracy of CAD Tools.
4. Initiate research work on designing methods to obtain accurate solutions.
5. Apply appropriate techniques, resources and tools to model devices for engineering activities to obtain fast and accurate designs.

DETAILED SYLLABUS:

UNIT I: BASIC COMPUTATION TOOLS (Periods: 15)
Linear systems and matrices – matrix formalities, condition of matrix systems, techniques for matrix solution, mixed boundary condition. Nonlinear Systems – scalar equations, matrix equations. Approximation, interpolation, curve fitting, Numerical Integration.

UNIT II:COMPUTATIONAL TOOLS FOR APPLICATIONS (Periods: 09)
Finite difference techniques, Initial Value problems, Energy Methods and Minimization, finite Element methods, dynamic methods in applied mechanics.

UNIT III: ADVANCED COMPUTATIONAL TOOLS (Periods: 08)
Method of characteristics – classification of partial Differential equations, Investigations in Engineering, Finite volume methods – Direct Analysis.

UNIT IV: GRID GENERATION AND ERROR ESTIMATES (Periods: 12)
Grid generation, Triangulation, errors and mesh Selection, Refinement Algorithms, Mesh Redistribution, Moving Grids.

UNIT V: APPLICATIONS TO DEVICE AND PROCESS SIMULATION (Periods: 11)
Applications to device and process simulation, Layout algorithms, Yield estimation algorithms, Symbolic analysis and Synthesis of Analog ICs.

Total periods: 55

TEXT BOOKS:

1. Herbert Koenig, "Modern Computational methods", CRC Press, 1988.
2. Graham F. Carey, "Computational Grids: generations, adaptation & Solution Strategies", CRC Press, 1997.
3. Naveed A. Sherwani, "Algorithms for VLSI Physical Design Automation", Kluwer Academic Publishers, 1993.

REFERENCE BOOK:

1. L.Pallage, R.Rohrer and C.Visweswaraiah, "Electronic Circuit and System Simulation Methods", McGraw Hill, 1995.

M. Tech. - I Semester
(16MT15703) DEVICE MODELING

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	4	-	-	4

PRE-REQUISITES:
A Course on Semiconductor Devices and Circuits at UG Level

COURSE OUTCOMES:
After successful completion of the course, students will be able to:
1. Gain in-depth knowledge in
   - Static and Dynamic Characteristics
   - Threshold Variations
   - Effects of MOS Layers
   - Modeling at low and High Frequencies.
2. Analyze complex engineering problems critically for conducting research in MOS device structures.
3. Solve engineering problems with wide range of solutions in different MOSFET technologies.
4. Initiate research methodologies in Modeling and Simulation of complex engineering activities in the field of VLSI Design at Circuit Level Implementation.
5. Apply appropriate techniques, resources and tools to engineering activities in modeling MOS structures.
6. Contribute positively to multidisciplinary scientific research in design and development of Integrated Circuits suited for wide range of applications.

DETAILED SYLLABUS:

UNIT-I (Periods: 12)
Basic Device Physics-I:
Two Terminal MOS Structure: Flat-band voltage, Potential balance & charge balance, Effect of Gate-substrate voltage on surface condition, Inversion, Small signal capacitance; C-V Characteristics.
Three Terminal MOS Structure: Contacting the inversion layer, Body effect, Regions of inversion, Pinch-off voltage.

UNIT-II (Periods: 14)
Basic Device Physics-II:
Four Terminal MOS Transistor: Transistor regions of operation, general charge sheet models, regions of inversion in terms of terminal voltage, strong inversion, weak inversion, moderate inversion, interpolation models, effective mobility, temperature effects, breakdown p-channel MOS FET, enhancement and depletion type, model parameter values, model accuracy .

UNIT-III (Periods: 14)
MOS Transistor with Ion-Implanted Channels: Enhancement of nMOS, Depletion nMOS, Enhancement pMOS.
Small dimension effects: Channel length modulation, barrier lowering, two dimensional charge sharing and threshold voltage, punch-through, carrier velocity saturation, hot carrier effects, scaling, effects of surface and drain series resistance, effects due to thin oxides and high doping. Sub threshold regions, Short channel effects.

UNIT-IV (Periods: 07)
MOS Transistor in Dynamic Operation: Large Signal modeling: Quasi static operation, Terminal currents in Quasi static operation, Evaluation of Charges in Quasi static operation, Transit time under DC conditions, Limitations of Quasi static Model, Non Quasi static Analysis.

UNIT-V **(Periods: 08)**

Small Signal Modeling for Low, Medium And High Frequencies: low, Medium frequency small signal model for the intrinsic part, Small signal model for Extrinsic Part, A complete Quasi static Model, Y-Parameter models, Non Quasi static Models.

Total Periods: 55

TEXT BOOK:

1. Y. Tsividis, "Operations and Modeling of the MOS Transistor", Oxford university Press, 3rd edition, 2012.

REFERENCE BOOKS:

1. Trond Ytterdal, Yuhua Cheng and Tor Fjeldly "Device Modeling for Analog and RF CMOS Circuit Design" Wiley Publication, 2003.
2. Donald A Neamen and Dhrubes Biswas "Semiconductor Physics and Devices" Special Indian Edition, 4th edition, 2012.

M. Tech. I - Semester
(16MT15704) DIGITAL IC DESIGN

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	4	-	-	4

PRE-REQUISITES:
A Course on Digital IC Applications and VLSI Design at UG Level.

COURSE DESCRIPTION:
Introduction to MOS transistors; Characteristics of CMOS digital circuits; Transistor sizing; memory design; Design strategies; Design of subsystems.

COURSE OUTCOMES:
After successful completion of the course, students will be able to:
1. Gain in-depth knowledge in
   - Static and dynamic characteristics of CMOS.
   - Alternative CMOS Logics
   - Transistor sizing
   - Adders Design
   - Design rules to develop layouts
   - Estimation of Delay and Power
2. Analyze complex engineering problems critically in the domain of CMOS Digital Integrated Circuits for conducting research.
3. Solve engineering problems for feasible and optimal solutions in the core area of CMOS Digital ICs.
4. Initiate research in Digital IC Applications.
5. Apply the Digital CMOS techniques for usage of modern CAD tools and their Limitations.
6. Contribute to multidisciplinary scientific work in the field of modern digital circuits like processor, memory designs.

DETAILED SYLLABUS:

UNIT I – CMOS INVERTER CHARACTERSTICS AND DESIGN STYLES (11 periods)

MOS INVERTERS: Introduction, Definitions and Properties, Static CMOS Inverter, Static and Dynamic Power Dissipation, CMOS inverter delay time definitions and calculations
DESIGNINGCOMBINATIONAL LOGIC GATES in CMOS: Introduction, Static CMOS Design, Dynamic CMOS Design, Domino and NORA logic, Power Consumption in CMOS Gates.

UNIT II – DESIGNING SEQUENTIAL LOGIC GATES in CMOS (12 periods)
Introduction, Static Sequential Circuits, Dynamic Sequential Circuits, Non-Bistable Sequential Circuit, Logic Style for Pipelined Structures.
Timing Issues in Digital Circuits: Introduction, Clock Skew and Sequential Circuit Performance, Clock Generation and Synchronization.

UNIT III – HIGH SPEED NETWORK AND MEMORY DESIGN (11 periods)
Methods of Logical Effort for transistor sizing -Power consumption in CMOS Gates, Low power CMOS design. CMOS Memory design – SRAM, DRAM.

UNIT IV – SUBSYSTEM DESIGN PROCESS (11 periods)
General arrangement of 4-bit Arithmetic Processor, Design of 4-bit shifter, Design of ALU sub-system, Implementing ALU functions with an adder, Multipliers, modified Booth's algorithm.

UNIT V – DESIGN METHODOLOGY AND TOOLS (10 periods)

Introduction, Structured Design Strategies, Design Methods, Design Flows, Design Economics, Data Sheets and Documentation.

Total Periods: 55

TEXT BOOKS:

1. Jan M Rabaey, "Digital Integrated Circuits", Pearson Education, 2nd Edition, 2003.
2. Sung-Mo Kang & Yusuf Leblebici, "CMOS Digital Integrated Circuits" McGraw Hill, 3rd edition, 2003.
3. Kamran Eshranghian, Douglas A. Puknell and Sholeh Eshranghian "Essential of VLSI Circuits and Systems", PHI, 1st edition, 2005.
4. Neil H. E. Weste, David Money Harris, "CMOS VLSI Design-A Circuit and Systems Perspective", Pearson Education, 4th Edition, 2011.

REFERENCE BOOKS:

1. Eugene D. Fabricus, "Introduction to VLSI Design", McGraw-Hill International Edition, 1990.
2. John P. Uyemura, "Introduction to VLSI Circuits and Systems", John Wiley & Sons, 2002.

M. Tech. - I Semester
(16MT15705) IC FABRICATION

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	4	-	-	4

PRE-REQUISITES:
A Course on Engineering Physics, Engineering Chemistry, Material Science, VLSI Design at UG Level

COURSE DESCRIPTION:
IC Fabrication process - Crystal growth, Wafer preparation, Epitaxial growth, Oxidation, Lithography, Etching, Deposition, Ion- Implantation, Metallization and Packaging of VLSI devices.

COURSE OUTCOMES:
After successful completion of the course, students will be able to:
1. Demonstrate in-depth knowledge in
   - Wafer preparation.
   - Lithography and Etching.
   - Diffusion process.
   - Assembly Techniques and Packaging.
2. Analyze IC fabrication methodologies and evaluate component effects on IC design for VLSI and ULSI domain.
3. Solve engineering problems by proposing potential solutions leading to better IC chip designs.
4. Initiate research in IC fabrication
5. Contribute to multidisciplinary scientific work in the field of Low power IC Fabrication.
6. Apply appropriate techniques to complex engineering activities in the field of VLSI Technology.

DETAILED SYLLABUS

UNIT-I: CRYSTAL GROWTH, WAFER PREPARATION, EPITARY AND OXIDATION. (13 Periods)
Clean room and safety requirements, Electronic grade silicon, Czochralski crystal growing, silicon shaping, Vapour phase Epitaxy, Molecular beam epitaxy, Epitaxial Evaluation, Growth mechanism and kinetics, Thin oxides, Oxidation Techniques and systems, Oxide properties, Redistribution of dopants at interface, Oxidation of polysilicon, Oxidation induced effects.

UNIT- II: LITHOGRAPHY AND REACTIVE PLASMA ETCHING (12 Periods)
Mask Making, Optical lithography, Electron lithography, X-ray lithography, Ion lithography, Plasma properties, Feature size control and Anisotropic Etch mechanism, Properties of Etch Processes, Reactive plasma etching Techniques and Equipments, Specific Etch Processes.

UNIT- III: DEPOSITION, DIFFUSION, ION IMPLANTATION (10 Periods)
Deposition process, polysilicon, Plasma Assisted deposition, models of diffusion in solids, Fick's one dimensional diffusion equation, Atomic diffusion mechanism, measurement techniques, Range theory, Implantation equipment, Annealing, Shallow junctions, High Energy Implantation.

UNIT- IV: METALLIZATION (10 Periods)
Metallization applications, Metallization choices, Physical Vapor Deposition, Patterning, Metallization problems, New role of metallization, Metallization systems, sputtering, problems associated with Al – Cu interconnect, Comparison of RC delay of Polysilicon.

UNIT- V: ANALYTICAL, ASSEMBLY TECHNIQUES & PACKAGING OF VLSI DEVICES (10 periods)

Analytical beams, Beams specimen interaction, Chemical methods, package types, packing design considerations, VLSI assembly technology, Package Fabrication Technology.

Total periods: 55

TEXT BOOKS:

1. S. M. Sze "VLSI Technology", Tata McGraw -Hill, 2nd edition, 1988.
2. Sorab. K. Gandhi "VLSI Fabrication and Principles", John Wiley & Sons, 2nd Edition, 1994.

REFERENCES BOOKS:

1. Amar Mukherjee "Introduction to NMOS & CMOS VLSI system Design", Prentice Hall, 1st Edition, 1986.
2. Mccanny and J.C.White "VLSI Technology and design", Academic Press, 1987.
3. Dasgupta "VLSI Technology", Pearson Education Pvt Ltd, 2001.

M.Tech. – I Semester
(16MT23808) REAL TIME SYSTEMS
(PE-I)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	4	-	-	4

PRE-REQUISITES:
Courses on Digital system design, Operating systems and embedded systems.

COURSE DESCRIPTION:
Real time system reference model; Real time scheduling approaches; Fault tolerant real time systems; Real time operating system concepts; Commercial RTOS.

COURSE OUTCOMES:
After successful completion of the course, students will be able to:
1. Demonstrate advanced knowledge in
   - Characterizing Real Time Systems
   - Various Scheduling approaches
   - Fault tolerant techniques
   - Real Time Operating System Services
2. Analyze critically various Operating Systems using Contemporary bench marks.
3. Consider trade-offs in Real Time System designing to solve engineering problems to exhibit specific behavior, given a set of performance goals and technology.
4. Familiarize with fault tolerant and scheduling techniques to overcome ever increasing embedded system design complexity combined with reduced time-to-market window to revolutionize embedded system design process.
5. Initiate research in Real Time Systems.
6. Explore tools and derive pseudo code using RTOS, for developing efficient embedded Systems.
7. Carry out multidisciplinary research in designing RTOS based systems.

DETAILED SYLLABUS:

UNIT-I: REAL TIME SYSTEMS (Periods: 10)
Hard Vs Soft Real Time Systems, a Reference Model of Real Time Systems- Processors and Resources, Temporal Parameters of Real Time Workload, Periodic Task Model, Precedence Constraints and Data Dependency. Functional Parameters, Resource Parameters of Jobs and Parameters of Resources, Scheduling hierarchy.

UNIT-II: APPROACHES TO REAL TIME SCHEDULING (Periods: 10)
Clock Driven, Weighted Round Robin, Priority Driven, Dynamic Vs Static Systems, Effective Release Times and Dead Lines, Optimality and Non-optimality of EDF and LST algorithms, Challenges in Validating Timing Constraints in Priority Driven Systems, Offline Vs Online Scheduling.

UNIT-III: (Periods: 12)
Scheduling Real Time Tasks in Multiprocessor and Distributed Systems: Multiprocessor task allocation, Dynamic allocation of tasks, Fault tolerant scheduling of tasks, Clocks in distributed Real Time Systems.
Fault Tolerance Techniques: Introduction, Failures- Causes, Types, Detection. Fault and Error Containment, Redundancy- Hardware, Software, Time. Integrated Failure Handling.

UNIT-IV: OPERATING SYSTEMS (Periods: 12)
Overview- Threads and Tasks, the Kernel. Time Services and Scheduling Mechanisms, Basic Operating System Functions- Communication and Synchronization, Event Notification and Software Interrupt Memory Management, I/O and Networking.

Processor Reserves and Resource Kernel, Capabilities of Commercial Real Time Operating Systems.

UNIT-V: COMMERCIAL REAL TIME OPERATING SYSTEMS (Periods: 12)

UNIX as RTOS - non preemptive kernel, Dynamic Priority levels and deficiencies. UNIX based Real Time Operating Systems - Extension to UNIX kernel, Host Target Approach, Preemption Point Approach, Self host systems. Windows as RTOS- features of Windows NT, Shortcomings, Windows NT vs UNIX. POSIX - Open software, Genesis of POSIX, Overview of POSIX, Real Time POSIX standard. Survey of Contemporary Real Time Operating Systems- PSOS, VRTX, VXworks, QNX, µC/OS-II, RT Linux, Lynx, Windows CE. Bench-marking Real Time Systems.

Total Periods: 56

TEXT BOOKS:

1. Jane W.S. Liu, "Real Time Systems", Pearson Education, 1st edition, April 2000.
2. C. M. Krishna, Kang G Shin, "Real Time Systems", McGraw-Hill Higher education, 1997.
3. Rajib Mall, "Real Time Systems-Theory and Practice", Pearson Education India, 1st edition, Nov.2012.

REFERENCE BOOKS:

1. Phillip A. Laplante and Seppo J. Ovaska, "Real-Time Systems Design and Analysis: Tools for the Practitioner", Wiley-IEEE Press, 4th edition, Nov. 2011.
2. Hermann Kopetz, "Real-Time Systems: Design Principles for Distributed Embedded Applications ", Springer; 2nd edition, 2011.

I M. Tech. – I Semester
(16MT15706) ADVANCED DIGITAL SIGNAL PROCESSING
(Common to VLSI (PE – I) & CMS)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	4	-	-	4

PRE-REQUISITES: Courses on Digital Signal Processing at UG level

COURSE DESCRIPTION:
Digital filter banks; Parametric and Non-Parametric Power Spectrum Estimation methods; computationally efficient algorithms; Applications of DSP.

COURSE OUTCOMES:
After successful completion of the course, students will be able to:
1. Gain in-depth knowledge in
   - Filter banks and Wavelets
   - Linear Prediction
   - Efficient power Spectral Estimation Techniques
   - Applications of Multirate signal processing
2. Analyze complex engineering problems critically in the field of Signal Processing.
3. Design optimum filters, multirate DSP systems and computationally efficient DSP algorithms for societal needs.
4. Solve engineering problems for feasible and optimal solutions in the field of digital signal processing.
5. Initiate research in advanced digital signal processing.
6. Learn and apply appropriate techniques, including prediction and modeling to complex engineering activities with an understanding of the limitations.
7. Contribute to scientific research in Radar signal processing ,Inter disciplinary areas like Speech and Image processing and Remote sensing with objectivity and rational analysis.

DETAILED SYLLABUS:

UNIT-I: MULTIRATE FILTER BANKS (Periods:12)
Decimation, Interpolation, Sampling rate conversion by a rational factor I/D, Multistage Implementation of sampling rate conversion. **Digital Filter Banks**: Two-Channel Quadrature-Mirror Filter Bank, Elimination of aliasing, condition for Perfect Reconstruction, Polyphase form of QMF bank, Linear phase FIR QMF bank, IIR QMF bank, Perfect Reconstruction Two-Channel FIR QMF Bank.

UNIT-II: POWER SPECTRAL ESTIMATIONS (Periods:12)
Estimation of spectra from finite duration observation of signals.

Non-Parametric Methods: Bartlett, Welch, Blackman & Tukey methods. Performance Characteristics of Non-parametric Power Spectrum Estimators, Computational Requirements of Non-parametric Power Spectrum Estimates.

Parametric Methods of Power Spectral Estimation:
Auto correlation & Its Properties, Relationship between auto correlation & model parameters, Yule-Walker & Burg Methods, MA & ARMA models for power spectrum estimation.

UNIT-III: LINEAR PREDICTION (Periods:10)
Forward and Backward Linear Prediction – Forward Linear Prediction, Backward Linear Prediction, Optimum reflection coefficients for the Lattice Forward and Backward Predictors. Solution of the Normal Equations: Levinson Durbin Algorithm, Schur Algorithm. Properties of Linear Prediction Filters.

UNIT-IV: DSP ALGORITHMS (Periods:10)

Fast DFT algorithms based on Index mapping, Sliding Discrete Fourier Transform, DFT Computation Over a narrow Frequency Band, Split Radix FFT, Linear filtering approach to Computation of DFT using Chirp Z-Transform.

UNIT-V: APPLICATIONS OF DIGITAL SIGNAL PROCESSING (Periods:11)

Digital cellular mobile telephony, Adaptive telephone echo cancellation, High quality A/D conversion for digital Audio, Efficient D/A conversion in compact hi-fi systems, Acquisition of high quality data, Multirate narrow band digital filtering, High resolution narrow band spectral analysis.

Total periods: 55

TEXT BOOKS:

1. John G. Proakis, Dimitris G. Manolakis, *Digital signal processing, principles, Algorithms and applications,* Prentice Hall, 4th edition, 2007.
2. Sanjit K Mitra, "*Digital signal processing, A computer base approach",* McGraw-Hill Higher Education, 4th edition, 2011.

REFERENCE BOOKS:

1. Emmanuel C Ifeacher Barrie. W. Jervis, "*DSP-A Practical Approach*", Pearson Education, 2nd edition, 2002.
2. A.V. Oppenheim and R.W. Schaffer, "*Discrete Time Signal Processing",* PHI, 2nd edition, 2006.

M. Tech. – I Semester
(16MT15707) FPGA ARCHITECTURES & APPLICATIONS
(PE - I)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	4	-	-	4

PRE-REQUISITES:
A Course on VLSI Design at UG Level.

COURSE DESCRIPTION:
Fundamentals of Programmable devices; Logic Implementation using PLDs and FPGAs.

COURSE OUTCOMES:
After successful completion of the course, students will be able to:
1. Demonstrate advanced knowledge in
   - Programmable Logic Devices
   - Different FPGA Architectures
   - Digital Implementation using FPGA
   - FPGA Applications
2. Analyze complex problems critically for digital implementation issues, to conduct research in Digital VLSI Design.
3. Solve engineering problems with wide range of solutions in FPGA Implementation.
4. Initiate research methodologies in Modeling, Simulation and Implementation of complex engineering applications in the field of Digital Design at different levels of abstraction.
5. Apply appropriate techniques, Resources and tools in, Modeling complex engineering applications with an understanding of limitations.
6. Contribute to multidisciplinary scientific work in the field of FPGA Devices.

DETAILED SYLLABUS

UNIT–I: **Programmable logic Devices** **(Periods: 08)**
Programmable logic Devices: ROM, PLA, PAL, CPLD, FPGA Features, Architectures and Programming, Applications and Implementation of MSI circuits using Programmable logic Devices.

UNIT – II: FPGAs **(Periods: 12)**
Field Programmable Gate Arrays- Logic blocks, routing architecture, design flow, technology mapping for FPGAs, Case studies Xilinx XC4000 & ALTERA's FLEX 8000/10000 FPGAs, Introduction to advanced FPGAs-Xilinx Virtex and ALTERA Stratix

UNIT -III: **(Periods: 14)**
Finite State Machines (FSM): Top Down Design, State Transition Table, State assignments for FPGAs, Realization of state machine charts using PAL, Alternative realization for state machine charts using microprogramming, linked state machine, encoded state machine.
FSM Architectures: Architectures centered around non registered PLDs, Design of state machines centered around shift registers, One Hot state machine, Petrinets for state machines-Basic concepts and properties, Finite State Machine-Case study.

UNIT – IV: System Level Design: **(Periods: 12)**
Controller, data path designing, Functional partition, Digital front end digital design tools for FPGAs. System level design using mentor graphics/Xilinx EDA tool (FPGA Advantage/Xilinx ISE), Design flow using FPGAs.

UNIT – V: Case studies **(Periods: 09)**

Design considerations using FPGAs of parallel adder cell, parallel adder sequential circuits, counters, multiplexers, parallel controllers

Total periods: 55

TEXT BOOKS:

1. Stephen M. Trimberger, "Field Programmable Gate Array Technology", Kluwer Academic Publications, 1994.
2. Richard F. Tinder, "Engineering Digital Design", Academic Press, 2nd edition, 2000.
3. Charles H. Roth, "Fundamentals of logic design", Thomson/Brooks/Cole, 5th edition, 2004.

REFERENCE BOOKS:

1. Pak K. Chan & Samiha Mourad, "Digital Design Using Field Programmable Gate Array", PTR Prentice Hall, 1st edition, 1994.
2. Stephen D. Brown, Robert J. Francis, Jonathan Rose, Zvonko G. Vranesic, "Field Programmable Gate Array", Kluwer Academic Publishers, 1st edition, 1992.

M. Tech. – I Semester
(16MT15708) RFIC DESIGN
(PE - I)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	4	--	--	4

PRE-REQUISITES:
A Course on Analog IC Design at UG Level/ PG Level.

COURSE DESCRIPTION:
Basic Concepts of RF Circuits; Transceiver Architectures; Low Noise Amplifier; Mixers; Oscillators; Power Amplifiers and Phased Locked Loops.

COURSE OUTCOMES:
After successful completion of the course, students will be able to:
1. Demonstrate in-depth knowledge in RFIC
   - Basic Concepts.
   - Transceiver Architectures.
   - Low Noise Amplifiers.
   - Mixers.
   - Voltage Controlled Oscillators.
   - Phase Locked Loop.
   - Power Amplifiers.
2. Analyze the problems in Radio Frequency Integrated Circuits.
3. Solve problems in transceiver architectures.
4. Initiate research work on designing RF systems for the wireless communications.
5. Apply appropriate techniques to overcome problem of non-idealities in the design of RFIC circuits, Implement various techniques to arrive at Efficient Designs of RFIC Circuits and Model techniques for Linearization of devices used in RFICs.

DETAILED SYLLABUS

UNIT – I: BASIC CONCEPTS IN RF DESIGN (Periods: 07)
Introduction to RF Design, Units in RF design, Time Variance and Nonlinearity, Effects of nonlinearity, random processes and Noise, Definitions of sensitivity and dynamic range, Passive impedance transformation, Scattering parameters.

UNIT – II: TRANSCEIVER ARCHITECTURES (Periods: 14)
General considerations, Receiver Architectures-Basic Heterodyne receivers, Modern heterodyne receivers, Direct conversion receivers, Image-Reject receivers, Low-IF receivers. Transmitter Architectures-Direct Conversion transmitters, Modern direct conversion Transmitters, Heterodyne Transmitters, Other Transmitter Architectures.

UNIT -III: LNA AND MIXERS (Periods: 10)
General considerations, Problem of input matching, Low Noise Amplifiers design in various topologies, Gain Switching, Band Switching, Mixers-General considerations, Passive down conversion mixers, Active down conversion mixers, Up conversion mixers.

UNIT – IV: OSCILLATORS (Periods: 10)
Performance parameters, Basic principles, Cross coupled oscillator, Three point oscillators, Voltage Controlled Oscillators, LC VCOs with wide tuning range, phase noise, Mathematical model of VCOS, Quadrature Oscillators.

UNIT – V: PLL AND POWER AMPLIFIER (Periods: 14)

PLLS-Phase detector, Type-I PLLs, Type-II PLLs, PFD/CP Non-idealities, Phase noise in PLLs, Loop Bandwidth. Power Amplifiers-General considerations, Classification of power amplifiers, High- Efficiency power amplifiers, Cascode output stages, Large signal impedance matching, Linearization techniques, Polar Modulation, Outphasing.

Total periods: 55

TEXT BOOK:

1. Behzad Razavi, "RF Microelectronics", PTR Prentice-Hall, 2nd edition, 1998.

REFERENCE BOOKS:

1. Thomas H. Lee, "The Design of CMOS Radio-Frequency Integrated Circuits", Cambridge University Press, 2nd edition, 1998.
2. R. Jacob Baker, Harry W. Li, D.E. Boyce, "CMOS Circuit Design, Layout and Simulation", Wiley, 1997.

.

M. Tech. - I Semester
(16MT15731) ANALOG IC DESIGN LAB

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
50	50	100	--	--	4	2

PRE-REQUISITES:
A Course on Linear IC Applications at UG Level.

COURSE DESCRIPTION:
Modeling and simulation of analog circuits using SPICE.

COURSE OUTCOMES:
After successful completion of the course, students will be able to:
1. Demonstrate knowledge in design of analog circuits.
2. Exhibit skills in SPICE Coding and verification of analog circuits.
3. Solve problems in Modeling and analysis of MOSFETs and OPAMPs.
4. Develop Skills to solve problems of design and analysis of analog circuits.
5. Initiate research in analog IC design.
6. Able to use CAD Tools to arrive at an optimized solution for analog signal design.
7. Contribute positively to multidisciplinary scientific research in design and development of Analog Integrated Circuits to solve problems arising in Integrated circuit Technology.
8. Communicate effectively in Verbal and written form of designs developed.

LIST OF EXERCISES:

Modeling and simulation of Analog Circuits using SPICE

1. Study of MOS Characteristics and Characterization.
2. Design and Simulation of single ended and differential Amplifiers.
3. Design and Simulation of Single Stage Amplifiers (Common Source, Source Follower, Common Gate Amplifier).
4. Design and Simulation of Single Stage Amplifiers (Cascode Amplifier, Folded Cascode Amplifier).
5. Design and Simulation of a Differential Amplifier (with Resistive Load, Current Source Biasing).
6. Design and Simulation of Basic Current Mirror, Cascode Current Mirror and Active Current mirrors.
7. Analysis of Frequency response of various amplifiers (Common Source, Source Follower, Cascode, Differential Amplifier.
8. Design/Simulation/Layout of Telescopic Operational Amplifier/ Folded Cascode Operational Amplifier.
9. Design and Simulation of Switched Capacitor.
10. Design and Simulation of various types of first and second order active filters and its applications.
11. Design and Simulation of full wave precision rectifier using opamp.
12. Design and simulation of basic applications based on opamp.

Total Time Slots: 12

REQUIRED SOFTWARE TOOL:
1. Cadence/Synopsys/Mentor graphics Tools.

REFERENCE BOOKS:

1. B. Razavi, Design of Analog CMOS Integrated Circuits, McGraw Hill, 2001.
2. Ken Martin, Analog Integrated Circuit Design, Wiley Publications, 2002.
3. Analog IC Design Lab manual.

M. Tech. - I Semester
(16MT15732) DIGITAL IC DESIGN LAB

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
50	50	100	--	--	4	2

PRE-REQUISITES:
A Course on Digital IC Applications at UG Level.

COURSE DESCRIPTION:
Modeling, Simulation, Synthesis and Implementation of digital circuits using HDLs;

COURSE OUTCOMES:
After successful completion of the course, students will be able to:
1. Demonstrate advanced knowledge in design of digital circuits.
2. Exhibit analytical skills in
   - Behavioral system modeling: concurrency and event-driven simulation.
   - Digital design modeling using various styles (behavioral, structural and dataflow)
   - Designing Combinational and sequential circuits
   - Verifying the Functionality of Designed circuits using function Simulator
   - Checking for critical path time calculation
   - Placement and routing in FPGA
   - Implement digital designs on FPGA device for conducting research in the field of Digital Circuits.
3. Conceptualize and Solve problems in logic verification and timing calculation of Digital circuits.
4. Initiate research in digital IC design.
5. Acquire research skills in the domain of Digital Systems.
6. Create, develop and use modern CAD tools to analyze problems of RTL, Technology schematic, and system implementation.
7. Contribute positively to multidisciplinary scientific research in design and development of Digital Integrated Circuits to solve problems arising in Integrated circuit Technology.
8. Communicate effectively in Verbal and written forms for the designs developed.

LIST OF EXERCISES:

Modeling and Functional Simulation of the following digital circuits (with XilinX tools) using Verilog Hardware Description Languages

Part–I: Combinational Logic: Basic Gates, Multiplexer, Comparator, Adder/ Substractor, Multipliers, Decoders, Address decoders, parity generator, ALU

Part–II: Sequential Logic: D-Latch, D-Flip Flop, JK-Flip Flop, Registers, Ripple Counters, Synchronous Counters, Shift Registers (serial-to-parallel, parallel-to-serial), Cyclic Encoder / Decoder.

Part–III: Memories and State Machines: Read Only Memory (ROM), Random Access Memory (RAM), Mealy State Machine, Moore State Machine, Arithmetic Multipliers using FSMs

Part-IV: FPGA System Design: Demonstration of FPGA and CPLD Boards, Demonstration of Digital design using FPGAs and CPLDs. Implementation of Mini-Project on FPGA/CPLD

Total Time Slots: 12

REQUIRED SOFTWARE TOOL:

1. Xilinx10.1 ISE and Above for FPGA.

REFERENCE BOOKS:

1. Jan M. Rabaey, Anantha Chandrakasan, & Borivoje Nikolic, "Digital Integrated Circuits – A design perspective", Prentice Hall, 3rd Edition, 2008.
2. Digital IC Design Lab manual.

M. Tech. – I Semester
(16MT13808) RESEARCH METHODOLOGY
(Common to all M. Tech. Programs)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
-	-	-	-	2	-	-

PREREQUISITES: --

COURSE DESCRIPTION:

Overview of Research, research problem and design, various research designs, data collection methods, statistical methods for research, importance of research reports and its types.

COURSE OUTCOMES:
After successful completion of the course, students will be able to:
1. Acquire in-depth knowledge on
   a. Research design and conducting research
   b. Various data collection methods
   c. Statistical methods in research
   d. Report writing techniques.
2. Analyze various research design issues for conducting research in core or allied areas.
3. Formulate solutions for engineering problems by conducting research effectively in the core or allied areas.
4. Carryout literature survey and apply research methodologies for the development of scientific/technological knowledge in one or more domains of engineering.
5. Select and Apply appropriate techniques and tools to complex engineering activities in their respective fields.
6. Write effective research reports.
7. Develop attitude for lifelong learning to do research.
8. Develop professional code of conduct and ethics of research.

DETAILED SYLLABUS:

Unit-I: Introduction to Research Methodology (Periods: 5)
Objectives and Motivation of Research, Types of Research, Research Approaches, Research Process, Criteria of good Research, Defining and Formulating the Research Problem, Problem Selection, Necessity of Defining the Problem, Techniques involved in Defining a Problem.

Unit-II: Research Problem Design and Data Collection Methods (Periods: 7)
Features of Good Design, Research Design Concepts, Different Research Designs, Different Methods of Data Collection, Data preparation: Processing Operations, Types of Analysis.

Unit-III: Statistics in Research (Periods:6)
Review of Statistical Techniques - Mean, Median, Mode, Geometric and Harmonic Mean, Standard Deviation, Measure of Asymmetry, ANOVA, Regression analysis.

Unit-IV: Hypothesis Testing **(Periods: 7)**

Normal Distribution, Properties of Normal Distribution, Basic Concepts of Testing of Hypothesis, Hypothesis Testing Procedure, Hypothesis Testing: t-Distribution, Chi-Square Test as a Test of Goodness of Fit.

Unit-V: Interpretation and Report Writing **(Periods: 3)**

Interpretation – Techniques and Precautions, Report Writing – Significance, Stages, Layout, Types of reports, Precautions in Writing Reports.

Total Periods: 28

TEXT BOOK:

1. C.R. Kothari, "*Research Methodology: Methods and Techniques*," New Age International Publishers, New Delhi, 2nd Revised Edition, 2004.

REFERENCE BOOKS:

1. Ranjit Kumar, "*Research Methodology: A step-by-step guide for beginners*," Sage South Asia, 3rd ed., 2011.
2. R. Panneerselvam, "Research Methodology," PHI learning Pvt. Ltd., 2009

M. Tech. – II Semester
(16MT25701) LOW POWER VLSI DESIGN

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	4	-	-	4

PREREQUISITE:
A Course on VLSI Design at UG Level.

COURSE DESCRIPTION:
Low Power Design Limitations; SOI and MOS/BICMOS Processes; Deep submicron processes; Integration/Isolation Considerations; CMOS/Bi-CMOS and Advanced Bi-CMOS Logic Gates; Design and Quality Measures of Low Power Latches & Flip-Flops; Special Low Power Techniques.

COURSE OUTCOMES:
After successful completion of the course, students will be able to:
1. Demonstrate in-depth knowledge in
    - Limitations of Low Power Design.
    - SOI Technology.
    - BiCMOS Processes.
    - MOSFET and BJT Behavior and Modeling.
    - BiCMOS Logic Gates Design.
    - Special low power techniques.
1. Analyze the low power BiCMOS circuits, the effects of devices and judge independently the best suited device for fabrication of smart devices for conducting research in ULSI design.
3. Solve problems of Low power design challenges, tradeoff between area, speed and power requirements.
4. Initiate research in low power VLSI design.
5. Apply appropriate techniques, resources and tools to engineering Activities in low power VLSI circuits.
6. Contribute to multidisciplinary scientific work in the field of low power Circuits.

DETAILED SYLLABUS:

UNIT –I: LOW POWER DESIGN AND AN OVER VIEW (Periods: 14)
Introduction to low- voltage low power design, limitations, Silicon-on-Insulator.
MOS/BiCMOS Processes: Bi-CMOS processes, Integration and Isolation considerations, Integrated Analog/Digital CMOS Process.

UNIT –II: LOW-VOLTAGE/LOW POWER CMOS/ BICMOS PROCESSES (Periods: 11)
Deep submicron processes, SOI CMOS, lateral BJT on SOI, future trends and directions of CMOS/Bi-CMOS processes.

UNIT-III: CMOS AND BI-CMOS LOGIC GATES (Periods: 12)
Conventional CMOS and Bi-CMOS logic gates, Performance Evaluation.
Low-Voltage Low-Power Logic Circuits: Comparison of advanced Bi-CMOS Digital circuits. ESD-free Bi-CMOS.

UNIT-IV: LOW POWER LATCHES AND FLIP FLOPS (Periods: 11)
Evolution of Latches and Flip flops-quality measures for latches and Flip flops, Design perspective.

UNIT – V: SPECIAL TECHNIQUES **(Periods: 07)**

Power Reduction in Clock Networks, CMOS Floating Node,Low Power Bus, Delay Balancing, Low Power Techniques for SRAM.

Total Periods: 55

TEXT BOOKS:

1. Yeo Rofail/ Gohl (3 Authors), "CMOS/BiCMOS ULSI low voltage, low power", Pearson Education Asia, 1st Indian reprint, 2002.
2. Gary K. Yeap, "Practical Low Power Digital VLSI Design", KAP, 2002.

REFERENCE BOOKS:

1. Douglas A. Pucknell, Kamran Eshraghian, "Basic VLSI Design", Prentice Hall, 3rd Illustrated Edition, 1994.
2. J. Rabaey, "Digital Integrated circuits: A Design perspective", Pearson Education, 2nd Edition, 2003.

M. Tech. - II Semester
(16MT25702) MIXED SIGNAL DESIGN

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	4	-	-	4

PRE-REQUISITES:
A Course on Analog Design at UG Level.

COURSE DESCRIPTION:
Switched capacitor circuits - analysis and application; Design and characterization of Phase locked loops; Data converters – types; Design for different sampling rates.

COURSE OUTCOMES:
After successful completion of the course, students will be able to:
1. Gain in-depth knowledge in
   - Switched Capacitor Circuits
   - PLL
   - Data Converters – ADC and DAC
2. Analyze complex engineering problems critically for conducting research in Data Converters for Communication Systems.
3. Solve engineering problems with wide range of solutions to increase Data Rate of ADC and DAC.
4. Design a mixed signal system/subsystem for societal needs.
5. Initiate research in mixed signal design.
6. Apply appropriate techniques, resources and tools to engineering activities in development of Data Converters.
7. Contribute positively to multidisciplinary scientific research in design and development of Mixed Integrated Circuits suited for wide range of applications.

DETAILED SYLLABUS:

UNIT -I: SWITCHED CAPACITOR CIRCUITS (Periods: 14)
Introduction to analog VLSI and mixed signal issues in CMOS technologies,Trade-offs in mixed signal design,Introduction to Switched Capacitor circuits- basic building blocks, Operation and Analysis, Non-idealeffects in switched capacitor circuits, Switched capacitor integrators first order filters, Switch sharing,Biquad filters.

UNIT -II: PHASED LOCK LOOP (PLL) (Periods: 10)
Basic PLL topology, Dynamics of simple PLL, Charge pump PLLs-Lock acquisition, Phase/Frequency detector and charge pump, Basic charge pump PLL, Non-ideal effects in PLLs-PFD/CP non-idealities, Jitter in PLLs, Delay locked loops, applications.

UNIT -III: DATA CONVERTER FUNDAMENTALS (Periods: 15)
DC and dynamic specifications, Quantization noise, performance limitations,Nyquist rate D/A converters- Decoder based Converters, Binary-Scaled converters, Thermometer-code converters, Hybrid converters.

UNIT -IV: NYQUIST RATE A/D CONVERTERS (Periods: 07)
Successive approximation converters, Flash converter, Two-step A/D converters, Interpolating A/D Converters, Folding A/D converters, Pipelined A/D converters, Time-Interleaved Converters.

UNIT -V: OVERSAMPLING CONVERTERS (Periods: 09)
Noise shaping modulators, Decimating filters and interpolating filters, Higher order modulators, Delta sigma modulators with multibit quantizers, Delta sigma D/A.

Total Periods: 55

TEXT BOOKS:

1. David A. Johns,Ken Martin, "Analog Integrated Circuit Design", Wiley Student Edition, 1997.
2. Behzad Razavi, "Design of Analog CMOS Integrated Circuits", Tata McGraw Hill Edition, 2001.
3. Philip E. Allen and Douglas R. Holberg, "CMOS Analog Circuit Design", Oxford University Press, 3rd Edition, 2012.

REFERENCE BOOKS:

1. Rudy Van De Plassche, "CMOS Integrated Analog-to-Digital and Digital-to-Analog converters", Springer US, 2nd Illustrated Edition, 2003.
2. Richard Schreier, "Understanding Delta-Sigma Data converters", Wiley Interscience, 1st Edition, 2004.
3. R. Jacob Baker, "CMOS Mixed-Signal Circuit Design", John Wiley & Sons, 2002.

M.Tech. - II Semester
(16MT25703) NANOELECTRONICS

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	4	--	--	4

PRE-REQUISITES:
Courses on Basic Engineering Physics, Basic Engineering Chemistry and Electronic Devices at UG level.

COUSRE DESCRIPTION:
Introduction to wave particle nature and mechanics; Crystal structure of semiconducting material; Material for nanoelectronics; Different techniques of nanostructure fabrication; Nanostructure Characterization; Electron transport mechanism.

COURSE OUTCOMES:
After successful completion of the course, students will be able to:
1. Demonstrate advanced knowledge in
   - wave particle nature, wave mechanics,
   - crystal structure of semiconducting material
   - different techniques of nanostructure fabrication,
   - characterization of the nanostructure and electron in well
2. Analyze
   - Crystal structure of nanomaterials
   - Nanostructure based device
3. Design and develop new nanodevices for advanced technological applications.
4. Efficiently solve complex problems in the field of nanoelectronics.
5. Involve and resolve the future research challenges in the fields related to Nanoelectronics.
6. Contribute to multidisciplinary research in biotechnology, MEMS, other nanotechnology fields.

DETAILED SYLLABUS:

UNIT I -PARTICLES AND WAVE MECHANICS (periods: 10)
Introduction classical particles, classical waves, wave–particle duality, Wave mechanics, Schrodinger wave equation, wave mechanics of particles, atoms and atomic orbital's.

UNIT II - MATRIAL FOR NANOELECTRONICS (periods: 10)
Introduction, Semiconductors, Crystal structure and Crystal lattices: bonding in crystals, Electron energy bands, Semiconductor heterostructures, Lattice-matched and pseudomorphic heterostructure, Organic semiconductors, Carbon nanomaterials: nanotubes and fullerenes.

UNIT III - FABRICATION AND CHARACTERISATION OF NANOSTRUCTURES (periods: 12)
Bulk crystal and heterostructure growth, Nanolithography, etching, and other means for fabrication of nanostructures and nanodevices, Characterization techniques of nanostructures, Spontaneous formation and ordering of nanostructures, Nanocrystals and nanoclusters, Methods of nanotube growth, Chemical and biological methods for nanoscale fabrication, Fabrication of nanoelectromechanical systems.

UNIT IV - ELECTRON TRANSPORT AND TRADITIONAL LOW-DIMENSIONAL STRUCTURES (periods: 10)
Electron Transport In Nanostructures
Introduction, Time and length scales of the electrons in solids, Statistics of the electrons in solids and nanostructures, The density of states of electrons in nanostructures, Electron transport in nanostructures.

Electrons In Traditional Low-Dimensional Structures
Introduction, Electrons in quantum wells, Electrons in quantum wires, Electrons in quantum dots.

UNIT V -NANOELECTRONIC DEVICES (periods: 13)
General Properties, Resonant Tunneling Diode, Operating Principle and Technology, Applications in High Frequency and Digital Electronic, Circuits and Comparison with Competitive Devices, Quantum Cascade Laser, Operating Principle and Structure, Quantum Cascade Lasers in Sensing and Ultrafast Free, Space Communication Applications, Single Electron Transistor, Operating Principle, Technology, Applications, Carbon Nanotube Devices Structure and Technology, Carbon Nanotube Transistors.

Total Periods: 55

TEXT BOOKS:

1. V. Mitin, V. Kochelap, M. Stroscio, "Introduction to Nanoelectronics", Cambridge University Press (2008).
2. W.R.Fahrner, "Nanotechnology and Nanoelectronics – Materials, Devices, Measurement Techniques", Springer-Verlag Berlin, Germany (2005).

REFERENCE BOOKS:

1. Supriyo Datta, "Lessons from Nanoelectronics: A New Perspective on Transport", World Scientific Publishing Co. Pte. Ltd. 5 Toh Tuck Link, Singapore 596224, Vol. 1, (2012).
2. Bhushan, Bharat, "Springer Handbook of Nanotechnology", 2nd edition, 2006.

M. Tech. – II Semester
(16MT25704) PHYSICAL DESIGN AUTOMATION

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	4	-	-	4

PRE-REQUISITES:
A Course on VLSI Design and Digital IC Design at UG Level.

COURSE DESCRIPTION:
Basics of VLSI design; Layout optimization; Simulation and synthesis; Physical design of FPGAs and MCMs.

COURSE OUTCOMES:
After successful completion of the course, students will be able to:
1. Demonstrate in-depth knowledge in
   - Algorithmic graph theory
   - Tractable and Intractable problems
   - Layout compaction such as floor planning, placement and routing
   - Binary-Decision diagrams
   - Simulation and Synthesis in High level abstraction
   - FPGA and MCM technologies
2. Analyze problems arising in circuit implementation.
3. Design an Integrated circuit with high level synthesis.
4. Solve engineering problems and arrive at optimal solutions pertaining to design automation.
5. Initiate research in physical design automation.
6. Apply appropriate techniques to Model and Simulate complex engineering designs using FPGA and MCM's.
7. Contribute positively to multidisciplinary applications in the design and development of Integrated Circuits.
8. Understand ethical responsibility towards environment and society in the development of automated designs.

DETAILED SYLLABUS

UNIT–I: INTRODUCTION TO VLSI DESIGN METHODOLOGIES (Periods: 10)
Introduction to VLSI Design automation tools, Introduction to algorithmic graph theory, Computational Complexity, Tractable and Intractable problems, Combinational optimization.

UNIT – II: LAYOUT COMPACTION (Periods: 12)
Design rules, problem formulation, algorithms for constraint graph compaction, placement & partitioning algorithms. Floor planning concepts- shape functions and floor plan sizing, types of routing problems.

UNIT -III: SIMULATION AND SYNTHESIS (Periods: 10)
Gate Level Modeling and Simulation, Switch Level Modeling and Simulation.
Basic issues and Terminology, Binary-Decision diagrams, Two-Level logic Synthesis.

UNIT – IV: HIGH LEVEL SYNTHESIS (Periods: 11)
Hardware modeling, internal representation of the input algorithm, allocation, assignment and scheduling algorithms, ASAP scheduling, Mobility based scheduling, list scheduling & force-directed scheduling.

UNIT–V: PHYSICAL DESIGN AUTOMATION OF FPGAs & MCMs (Periods: 12)
FPGA technologies, Physical Design cycle for FPGAs, partitioning and Routing for segmented and staggered Models, MCM technologies, MCM physical design cycle, Partitioning, Placement- Chip Array based and Full Custom Approaches, Routing, Maze routing, Multiple stage routing, Routing and Programmable MCMs.

Total Periods: 55

TEXT BOOKS:

1. S.H.Gerez, "Algorithms for VLSI Design Automation", John Wiley & Sons Pvt. Ltd, 2nd Edition, 1999.
2. Naveed Sherwani, "Algorithms for VLSI Physical Design Automation", Springer International Edition, 3rd edition, 2005.

REFERENCE BOOKS:

1. Hill & Peterson, "Computer Aided Logical Design with Emphasis on VLSI", John Wiley & Sons Pvt. Ltd, 4th edition, 1993.
2. Wayne Wolf, "Modern VLSI Design Systems on silicon", Pearson Education Asia, 2nd Edition, 1998.

M. Tech. - II Semester
(16MT25705) TESTING AND TESTABILITY

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	4	-	-	4

PREREQUISITE:
A Course on Digital Logic Design at UG Level.

COURSE DESCRIPTION:
Design for testability; Fault modeling and simulation; Test analysis for digital circuits; Design strategies for testability.

COURSE OUTCOMES:
After successful completion of the course, students will be able to:
1. Demonstrate advanced knowledge in
   - The basic faults that occur in digital systems
   - Testing of stuck at faults for digital circuits
   - Design for testability
2. Analyze testing issues in the field of digital system design critically for Conducting Research.
3. Solve engineering problems by modeling different faults for fault free Simulation in Digital circuits.
4. Apply appropriate research methodologies to develop New testing Strategies for digital and mixed signal circuits and systems.
5. Apply appropriate techniques, Resources and tools in, Modeling to Complex Engineering activities with an understanding of the limitations.
6. Contribute to multidisciplinary scientific work in the field of testing of Stuck at Faults for digital circuits.

DETAILED SYLLABUS:

UNIT –I: INTRODUTION TO TEST AND DESIGN FOR TESTABILITY (Periods: 13)
Modeling-Modeling Digital Circuits at Logic Level, Register Level and Structural Models. Level of Modeling, Logic Simulation- Types of Simulation, Delay Models, Element Evaluation, Hazard Detection, Gate Level Event Driven Simulation.

UNIT–II: FAULT MODELLING (Periods: 09)
Logic Fault Models, Fault Detection and Redundancy, Fault Equivalence and Fault Location, Fault Dominance, the Single Stuck-Fault Model, The Multiple Stuck-Fault Model.

UNIT-III: FAULT SIMULATION (Periods: 07)
Applications, General Fault Simulation Techniques, Fault Simulation for Combinational Circuits, Fault Sampling.

UNIT-IV: TESTING FOR SINGLE STUCK FAULTS (Periods: 12)
ATG for SSSFs in Combinational Circuits and Sequential Circuits, Testing for bridging faults, Functional Testing With Specific Fault Models, Vector Simulation- ATPG Vectors, Formats Compaction and Compression, Selecting ATPG Tool.

UNIT–V: DESIGN FOR TESTABILITY (Periods: 14)
Testability Trade Offs, Techniques, Scan Architectures and Testing, Controllability and Observability by means of Scan Registers, Generic Scan-Based Designs, Full Serial Integrated Scan, Storage Cells for Scan Designs, Board-Level and System-Level DFT Approaches, Boundary Scans Standards, Compression Techniques, Different Techniques, Syndrome Testing and Signature Analysis, Introduction to BIST Concepts.

Total periods: 55

TEXT BOOKS:

1. MironAbramovici, Melvin A. Breur, Arthur D.Friedman, "Digital Systems Testing and Testable Design", Wiley, 1st Edition, 1994.
2. Alfred L. Crouch, "Design for Test for Digital ICs & Embedded Core Systems", Prentice Hall PTR, 1st Reprint Edition, 1999.

REFERENCE BOOK:

1. Robert J.Feugate, Jr., Steven M.McIntyre, "Introduction to VLSI Testing", Prentice Hall, 1st Illustrated Edition,1998.

M. Tech. – II Semester
(16MT13806) ASIC DESIGN
(PE-II)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	4	--	--	4

PRE-REQUISITES:
A Course on VLSI Design at UG Level.

COURSE DESCRIPTION:
ASIC design categories; Design Libraries; Design Entry; Logic Synthesis; Simulation; Testing; Physical design flow of ASIC.

COURSE OUTCOMES:
After successful completion of the course, students will be able to:
1. Gain in-depth knowledge in
   - ASIC Design Styles.
   - ASICs Design Libraries.
   - ASICs Design Issues.
   - ASIC Construction.
2. Analyze problems critically in the field of ASIC Design.
3. Design Application Specific ICs for use in various systems.
4. Solve engineering problems and arrive at optimal solutions in pertaining to ASIC Design.
5. Initiate research in ASIC Design.
6. Apply appropriate techniques, resources and tools to engineering activities to provide appropriate Solution for the development of ASICs.
7. Contribute to multidisciplinary scientific work in the field of ASIC Design.

DETAILED SYLLABUS:

UNIT-I: INTRODUCTION TO ASICs (Periods: 10)
Types of ASICs- Full-Custom ASICs, Semicustom ASICs, Standard cell based ASICs, Gate- array based ASICs, Channeled Gate Array, Channel less Gate Array, Structured Gate Array, Programmable Logic Devices, Field-Programmable Gate Arrays, ASIC Design Flow, ASIC Cell Libraries.

UNIT-II: ASIC LIBRARY DESIGN & PROGRAMMABLE ASICs (Periods: 10)
ASIC LIBRARY DESIGN: Transistors as Resistors, Transistor Parasitic Capacitance, Logical Effort, Library cell design, Library Architecture, Gate-Array Design, Standard-Cell Design, Data path-Cell Design.
PROGRAMMABLE ASICs: Anti fuse, Static RAM, EPROM and EEPROM technology, Practical Issues, Specifications.

UNIT-III: LOW-LEVEL DESIGN ENTRY & LOGIC SYNTHESIS (Periods: 12)
LOW-LEVEL DESIGN ENTRY: Schematic Entry, Hierarchical design, The cell library, Names, Schematic Icons & Symbols, Nets, Schematic Entry for ASICs, Connections, Vectored instances and Buses, Edit-in-place, Attributes, Net list Screener, Back-Annotation.
LOGIC SYNTHESIS: A Logic-Synthesis Example**,** Verilog and Logic Synthesis, VHDL and Logic Synthesis, Finite-State Machine Synthesis, Memory Synthesis.

UNIT-IV: SIMULATION, TESTING & ASIC CONSTRUCTION (Periods: 13)
SIMULATION AND TESTING: Types of Simulation -Structural Simulation, Gate-Level Simulation, Static Timing Analysis, Formal Verification, Switch-Level Simulation, Transistor-Level Simulation, Boundary Scan Test, Faults, Fault simulation, Automatic Test-Pattern Generation.

ASIC CONSTRUCTION: Physical Design, System Partitioning, FPGA Partitioning, Partitioning Methods.

UNIT-V: FLOOR PLANNING, PLACEMENT & ROUTING (Periods: 10)
FLOOR PLANNING AND PLACEMENT: Floor planning, Placement, Physical Design Flow, **ROUTING:** Global Routing, Detailed Routing, Special Routing, Circuit Extraction and DRC.

Total Periods: 55

TEXT BOOKS:

1. Micheal John Sebastian Smith, "Application - Specific Integrated Circuits", Addison Wesley Professional, 1997.
2. L. J. Herbst, "Integrated circuit engineering", Oxford University Press, 1996.

REFERENCE BOOKS:

1. Neil H.E. Weste, Kamran Eshraghian, "Principles of CMOS VLSI Design: A Systems Perspective", Addison – Wesley Publication Company, 2nd Edition, 1999.
2. John P. Uyemura, "Introduction to VLSI Circuits and Systems", Wiley, 1st Illustrated Edition, 2002.

M. Tech. – II Semester
(16MT25707) CO – DESIGN
(PE – II)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	4	-	-	4

PRE-REQUISITES:
Courses on Computer Architecture, Digital Design, Software Design, and Embedded Systems.

COURSE DESCRIPTION:
Issues and Algorithms in CO- Design; Prototyping and its Emulation on Target Architectures; Compilation Techniques; Design Specification; Verification Tools for Embedded Processor Architectures; System- Level Languages with its Specification and Design.

COURSE OUTCOMES:
After successful completion of the course, students will be able to:
1. Demonstrate advanced knowledge in
   - Various design steps starting from system specifications to hardware/software implementation
   - Process optimization techniques while considering various design decisions
2. Analyze complex problems critically in the domains of case studies using contemporary high-level methods, for conducting research in VLSI Design.
3. Solve engineering problems by considering trade-offs in the way hardware and software components of a system work together to exhibit a specific behavior for given a set of performance goals and technology with wide range of solutions in Real time embedded system design.
4. Apply appropriate research methodologies in Modeling and Simulation of complex engineering activities in the field of Real time embedded system design.
5. Apply appropriate techniques, Resources and tools in, Modeling to complex engineering activities with an understanding of the limitations
6. Contribute to multidisciplinary scientific work in the field of Real time embedded system design.
7. Understand ethical responsibility towards environment and society in the field of Real time embedded system design.

DETAILED SYLLABUS

UNIT–I: (Periods: 13)
CO-Design Issues: Co-design Models, Architectures, Languages, a Generic Co-design Methodology
Co-Synthesis Algorithms: Architectural Models, Hardware/Software Partitioning, Distributed System Co-Synthesis

UNIT – II: (Periods: 08)
Prototyping and Emulation: Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping
Target Architectures- I: Architecture Specialization techniques, System Communication infrastructure

UNIT -III: Target Architectures – II: (Periods: 07)
Target Architecture and Application System classes, Architecture for control dominated systems- 8051. Architectures for High performance control, Architecture for Data dominated systems- ADSP21060, TMS320C. Mixed Systems and Less Specialized Systems

UNIT – IV: **(Periods: 14)**

Compilation Techniques and Tools for Embedded Processor Architectures: Modern embedded architectures, embedded software development needs, compilation technologies, Practical consideration in a compiler development environment.

Design Specification and Verification: Design, co-design, the co-design computational model, concurrency, coordinating concurrent computations, interfacing components, Verification- Design verification and implementation verification, verification tools and interface verification.

UNIT–V: **(Periods: 13)**

Languages for System- Level Specification and Design: System Level Specification, Design Representation for System Level Synthesis, System Level Specification Languages, Heterogeneous Specifications and Multi Language Co-simulation- Concepts for Multi-language design , Co-simulation models.

The Cosyma Systems: Overview, Architecture- design flow and user interaction. Partitioning, Synthesis

Lycos System: Introduction, Partitioning and Design Space Exploration

Total periods: 55

TEXT BOOK:

1. Jorgen Staunstrup, Wayne Wolf, "Hardware / Software Co- Design Principles and Practice", Springer US, 2010.

REFERENCE BOOK:

1. Felice Balarin, .et .al, "Hardware-Software Co-Design of Embedded Systems: The POLIS Approach" Springer Science & Business Media, 2012.

M. Tech. - II SEMESTER
(16MT25708) SYSTEM-ON-CHIP DESIGN AND VERIFICATION
(PE – II)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	4	-	-	4

PREREQUISITE:
Courses on Embedded systems and VLSI design.

COURSE DESCRIPTION:
System on Chip Design Process; System level Design Issues; Test Strategies; Macro Design and Verification; Reusable Macros; System on Chip Verification; Communication Architectures for SoCs.

COURSE OUTCOMES:
After successful completion of the course, students will be able to:
1. Demonstrate in-depth knowledge in
    - System on Chip Design Processes.
    - Macro Level Design.
    - Verification Techniques.
    - On-Chip Communication Architectures.
    - Bus Functional Model based Verification.
2. Analyze the problems in SoC Design for Low Power Architecture Design.
3. Develop Skills to solve problems of Reusable Macros.
4. Initiate research work on Reusable Design for the development of SoC Architectures.
5. Implement various Verification techniques to arrive at Efficient Designs of SoC Architectures.

DETAILED SYLLABUS:

Unit-I: System on Chip Design Process (Periods: 08)
A canonical SoC Design, SoC Design flow- waterfall vs spiral, top down vs Bottom up. Specification requirement, Types of Specification, System Design process, System level design issues - Soft IP Vs Hard IP, Design for timing closure - Logic design issues, Verification strategy, Onchip buses and interfaces, Design for Low Power, Manufacturing test strategies.

Unit-II: Macro Design Process (Periods: 08)
Overview of IP Design, planning and Specification, Macro Design and Verification, Soft Macro Productization, Developing hard macros - Design issues for hard macros, Model Development for Hard Macros. System Integration with reusable Macros.

Unit-III: SoC Verification - I (Periods: 14)
Technology Challenges, Verification technology options, Verification methodology, Testbench Creation, Testbench Migration, Verification languages, Verification IP Reuse, Verification approaches, Verification and Device Test, Verification plans, Bluetooth SoC.
System level verification – System Design, System Verification.
Block level verification – IP Blocks, Block Details of Bluethooth SoC, Lint Checking, Formal Model Checking, Functional Verification/Simulation, Protocol Checking, Directed Random Testing, Code Coverage Analysis.

Unit-IV: SoC Verification - II (Periods: 15)
Hardware/Software Co-verification- HW/SW Co-verification Environment, Emulation, soft or virtual Prototypes, Co-verification, UART Co-verification, Rapid Prototype Systems, Software Testing. Static netlist verification, Physical Verification and Design Signoff, Introduction to VMM (Verification Methodology Manual), OVM(Open Verification Methodology) and UVM (Universal Verification Methodology).

Unit-V: Design of Communication Architectures for SoCs (Periods: 10)
On chip communication architectures, System level analysis for designing communication, Design space exploration, Adaptive communication architectures - Communication architecture tuners. Communication architectures for energy/battery efficient systems. Introduction to bus functional models and bus functional model based verification.

Total Periods: 55

TEXT BOOKS:

1. Michael Keating, Pierre Bricaud, "Reuse Methodology manual for System-On-A-Chip Designs", Kluwer Academic Publishers, 2nd Edition, 2002.
2. Prakash Rashinkar, Peter Paterson, Leena Singh, "SoC Verification Methodology and Techniques", Kluwer Academic Publishers, 2002.
3. Ahmed Amine Jerraya, Wayne Wolf, "Multiprocessor Systems-on-chips", Morgan Kaufmann Publishers, 2005.

REFERENCE BOOKS:

1. William K. Lam, "Hardware Design Verification: Simulation and Formal Method based Approaches", Prentice Hall Professional Technical Reference, 2005.
2. Farzad Nekoogar, Faranak Nekoogar, "From ASICs to SOCs: A Practical Approach", Prentice Hall Professional, 2003.

M. Tech. -II Semester
(16MT25709) WIRELESS SENSOR NETWORKS
(Common to VLSI & CMS)
(PE-II)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	4	-	-	4

PRE-REQUISITES: --
A Course on Computer Networks and Wireless Communication and Networks at UG Level.

COURSE DESCRIPTION:
WSN architecture, types, Quality measures of wireless channels, various MAC protocols, Sensor deployment and routing related protocols, congestion control in WSNs.

COURSE OUTCOMES:
After successful completion of the course, students will be able to:
1. Gain in-depth knowledge in
   - Wireless Sensor Networks
   - Physical layer
   - Data link layer
   - Network layer
   - Transport layer
2. Analyze various design issues for conducting research related to Datalink, network and transport protocols of wireless sensor network architecture.
3. Design and develop feasible and optimal solutions for societal use.
4. Solve complex engineering problems pertaining to the field of wireless sensor networks.

DETAILED SYLLABUS

UNIT – I: Introduction To Wireless Sensor Networks (10 Periods)
Challenges for wireless sensor networks, Comparison of sensor network with ad hoc network, Single node architecture - Hardware components, energy consumption of sensor nodes. Network architecture: Sensor network scenarios - types of sources and sinks, single hop versus multi-hop networks, multiple sinks and sources. Design principles for wireless sensor networks.

UNIT – II: Physical Layer (10 Periods)
Introduction, wireless channel and communication fundamentals – frequency allocation, modulation and demodulation, wave propagation effects and noise, channels models, spread spectrum communication, packet transmission and synchronization, quality of wireless channels and measures for improvement. Physical layer and transceiver design consideration in wireless sensor networks - Energy usage profile, choice of modulation, Power Management .

UNIT -III: Data Link Layer (16 Periods)
MAC protocols: fundamentals of wireless MAC protocols - Requirements and design constraints for wireless MAC protocols, Important classes of MAC protocols, MAC protocols for wireless sensor networks. Low duty cycle protocols and wakeup concepts - Sparse topology and energy management (STEM), S-MAC, Wakeup radio concepts. Contention-based protocols - CSMA protocols, PAMAS. Schedule-based protocols - SMAC, BMAC, Traffic-adaptive medium access protocol (TRAMA). Link Layer protocols – fundamentals task and requirements, error control - Causes and characteristics of transmission errors, ARQ techniques, FEC techniques, Hybrid schemes, Power control

UNIT – IV: Network Layer (10 Periods)

Gossiping and agent-based uni-cast forwarding - Basic idea, Randomized forwarding. Energy-efficient unicast, Broadcast and multicast - Source-based tree protocols, Shared, core-based tree protocols, Mesh-based protocols. geographic routing - Basics of position-based routing, Geocasting. Mobile nodes - Mobile sinks, Mobile data collectors, Mobile regions. Data centric and content-based networking - Introduction, Data-centric routing, Data aggregation.

UNIT – V: Transport Layer (09 Periods)

The transport layer and QoS in wireless sensor networks - Quality of service/reliabilitym, Transport protocols. Coverage and deployment - Sensing models, Coverage measures, Uniform random deployments: Poisson point processes, Coverage of random deployments: Boolean sensing model, general sensing model, Coverage determination, Coverage of grid deployments. Reliable data transport, Single packet delivery - Using a single path, Multiple paths, Multiple receivers. Congestion control and rate control - Congestion situations in sensor networks, Mechanisms for congestion detection and handling, Protocols with rate control, The CODA congestion-control framework.

Total periods: 55

TEXT BOOK:

1. Holger Karl, Andreas willig "Protocol and Architecture for Wireless Sensor Networks", John wiley publication, Oct 2007.

REFERENCE BOOKS:

1. Fengzhao, Leonidas, Guibas, "Wireless Sensor Networks: an information processing approach –publication, Elsevier,2004.
2. Edgar H .Callaway,"Wireless Sensor Networks: Architecture and protocol", 1st Edition, CRC press 2003.
3. C.S.Raghavendra Krishna, M.Sivalingam and Taribznati, "Wireless Sensor Networks", Springer publication, 2006.

M.Tech. – II Semester
(16MT25731) MIXED SIGNAL AND PHYSICAL DESIGN AUTOMATION LAB

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
50	50	100	-	-	4	2

PREREQUISITE:
A course on Circuit Level Design and Layouts.

COURSE DESCRIPTION:
Design and Verification of Analog and Mixed Signal Circuits.

COURSE OUTCOMES:
After successful completion of the course, students will be able to:
1. Demonstrate advanced knowledge in backend and frontend design.
2. Exhibit analytical skills in
    - Backend Design - Schematic or SPICE Entry, Simulation, Layout, DRC, PEX, Post Layout Simulation.
    - Frontend Design - HDL Design Entry, Logic Simulation, RTL Logic Synthesis, Post Synthesis Timing Simulation, Partition, Floorplanning, Place & Route, Compaction, Verification, Design for Testability, Static Timing Analysis, Power Analysis.
3. Solve problems in physical design cycle, functional verification, timing and Power Analysis of Digital circuits.
4. Initiate research in the field of mixed signal and physical design automation.
5. Develop Skills to solve problems of layout design and build solutions for optimizing design for area, power and speed.
6. Use CAD Tools to arrive at an optimized solution for mixed signal design.
7. Contribute positively to multidisciplinary scientific research in design and development of Mixed/Analog Integrated Circuits to solve problems arising in physical design and Integrated circuit Technology.
8. Communicate effectively in Verbal and written form of designs developed.

LIST OF EXERCISES:
Mentor Graphic tools / Cadence tools / Synopsis tools

1. **Backend Design** **(4 Slots)**
   Schematic Entry, Simulation, Layout, DRC, PEX, Post Layout Simulation of CMOS Logic Gates, Combinational Circuits (Adders, Encoders, Decoders, Multiplexers, Demultiplexers, etc), Sequential Circuits(Flip Flops, Registers, counters),Biquad Filter, PLL, VCO and ADC/DAC.

2. **Frontend/Semicustom Design** **(4 Slots)**
   HDL Design Entry, Logic Simulation, RTL Logic Synthesis, Post Synthesis TimingSimulation, Place & Route, Design for Testability, Static Timing Analysis, PowerAnalysis of Combinational and Sequential Circuits(Application Oriented designs – MAC Unit, FIR and IIR Filters, Traffic Light Controller, FSM based Control applications, etc).

3. **Physical Design Automation** **(4 Slots)**
   Graph Algorithms, Partitioning Algorithms, Floorplanning Algorithms, Routing Algorithms.

Total Time Slots: 12

Required Software Tools:
1. Mentor Graphic tools / Cadence tools / Synopsis tools/MAGMA/MAGIC. (220 nm Technology and Above)
2. Xilinx ISE 10.1i and Above for FPGA/CPLDS.

REFERENCE BOOKS:
1. Mixed Signal Laboratory Manual

M.Tech. - II Semester
(16MT25732) NANOELECTRONICS LAB

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
50	50	100	--	--	4	2

PRE-REQUISITES:
A course on Circuit Level Design

COUSRE DESCRIPTION:
Demonstration of the lab; Design, fabrication and verification of the nanoelectronic devices.

COURSE OUTCOMES:
After successful completion of the course, students will be able to:
1. Demonstrate advanced knowledge in
    - Clean room,
    - Substrate preparation
    - Device fabrication
    - Device characterization
    - Device verification
2. Able to analyze
    - Nanostructure of the Devices
    - New material and Device characterization
3. Think laterally to get involved efficiently in research field of nanoelectronics.
4. Efficiently solve complex problem in the design of nanoelectronic devices.
5. Design and develop new nanodevice for advance technological application.
6. Use tools for verifying developed nanodevices.
7. Communicate effectively in verbal and written form for the experiments.
8. Utilize and implement the practical knowledge in multidiscipline areas.

LIST OF EXERCISES:

Demonstration, fabrication and characterization of nano devices (8 Slots)

1. Clean room demonstration
2. Clean bench demonstration
3. Demonstration of substrate
4. Cleaning of substrate
5. Deposition of filter by sol-gel method
6. Deposition of thermal evaporation
7. Device fabrication
8. Device characterization

Verification of fabricated devices (4 Slots)

9. Verification of device characteristics using MATLAB
10. Verification of device characteristics using COMSOL.
11.

Total Time Slots: 12

REFERENCE BOOKS:

1. Nanoelectronics Lab Manual

M. Tech. - II Semester
(16MT25733) SEMINAR

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
-	100	100	-	-	-	2

PRE-REQUISITES: --

COURSE DESCRIPTION:
Identification of seminar topic; literature survey; preparation of technical report and presentation.

COURSE OUTCOMES:
After successful completion of the course, students will be able to:
1. Demonstrate knowledge to identify an advanced topic for seminar in core and allied areas of VLSI.

2. Extract and analyze information pertinent to the topic through literature survey.

3. Comprehend extracted information through analysis and synthesis critically.

4. Plan, prepare and present effective written and oral technical report on the work done.

5. Develop enthusiasm and commitment to engage in lifelong learning for technical competence in the field of VLSI.

6. Consider and assess the impact of the seminar topic outcome on environment and society.

7. Undertake corrective measures for both the technical and ethical mistakes.

M. Tech. – II Semester
(16MT23810) INTELLECTUAL PROPERTY RIGHTS
(Common to all M. Tech. Programs)
(Audit Course)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
-	-	-	-	2	-	-

PRE-REQUISITES: --

COURSE DESCRIPTION:

Introduction to Intellectual Property; Trade Marks; Law of Copy Rights; Law of Patents; Trade Secrets; Unfair Competition; New Development of Intellectual Property.

COURSE OUTCOMES:
After successful completion of the course, students will be able to:
1. Demonstrate in-depth knowledge on
   - Intellectual Property
   - Trade Marks & Secrets
   - Law of Copy Rights, Patents
   - New development of Intellectual Property
2. Analyze the different forms of infringement of intellectual property rights.
3. Solve problems pertaining to Intellectual Property Rights.
4. Stimulate research zeal for patenting of an idea or product.
5. Write effective reports required for filing patents.
6. Develop life-long learning capabilities.
7. Develop awareness of the relevance and impact of IP Law on their academic and professional lives.
8. Develop attitude for reflective learning.

DETAILED SYLLABUS:

UNIT - I: Introduction to Intellectual property (Periods:5)
Introduction, types of intellectual property, international organizations, agencies and treaties, importance of intellectual property rights.

UNIT - II: Trade Marks: (Periods:5)
Purpose and function of trademarks, acquisition of trade mark rights, protectable matter, selecting and evaluating trade mark, trade mark registration processes.

UNIT - III: Law of copy rights: (Periods:6)
Fundamental of copy right law, originality of material, rights of reproduction, rights to perform the work publicly, copy right ownership issues, copy right registration, notice of copy right, international copy right law.
Law of patents: Foundation of patent law, patent searching process, ownership rights and transfer

UNIT - IV: Trade Secrets: (Periods:6)
Trade secrete law, determination of trade secrete status, liability for misappropriations of trade secrets, protection for submission, trade secrete litigation.
Unfair competition: Misappropriation right of publicity, False advertising.

UNIT - V: New development of intellectual property: (Periods:6)

New developments in trade mark law; copy right law, patent law, intellectual property audits.

International overview on intellectual property, international - trade mark law, copy right law, international patent law, international development in trade secrets law.

Total Periods: 28

REFERENCE BOOKS:

1. Deborah, E. Bouchoux, *Intellectual property right*, Cengage learning.
2. Prabuddha ganguli, *Intellectual property right - Unleashing the knowledge economy*, Tata Mc Graw Hill Publishing Company Ltd.

M. Tech. - III & IV Semester
(16MT35731 & 16MT45731)PROJECT WORK

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
200	200	400	-	-	-	28

PRE-REQUISITES:--

COURSE DESCRIPTION:
Identification of topic for the project work; Literature survey; Collection of preliminary data; Identification of implementation tools and methodologies; Performing critical study and analysis of the topic identified; Time and cost analysis; Implementation of the project work; Writing of thesis and presentation.

COURSE OUTCOMES:
After successful completion of the course, students will be able to:
1. Demonstrate capacity to identify an advanced topic for project work in core and allied areas.
2. Extract information pertinent to the topic through literature survey.
3. Comprehend extracted information through analysis and synthesis critically on the topic.
4. Solve engineering problems pertinent to the chosen topic for feasible solutions.
5. Use the techniques, skills and modern engineering tools necessary for project work.
6. Do time and cost analysis on the project.
7. Plan, prepare and present effective written and oral technical report on the topic.
8. Adapt to independent and reflective learning for sustainable professional growth.
9. Contribute to multidisciplinary scientific work in the field of VLSI.
10. Understand ethical responsibility towards environment and society in the field of VLSI.
11. Engage lifelong learning for development of technical competence in the field of VLSI.