

SREE VIDYANIKETHAN ENGINEERING COLLEGE (AUTONOMOUS) Sree Sainath Nagar, A. Rangampet – 517 102

Department of Computer Science and Systems Engineering

Report on Expert lecture on Multicore Architectures

Dr. M. Rajasekhar Babu, Professor, Department of Computer Science, School of Computer Science, VIT University, Vellore., delivered an Expert lecture on "Multicore Architectures" for II B.Tech & III B.Tech of CSSE, Faculty of CSE, IT, CSSE and MCA students in ED-Cell on 24th January 2013.

Dr. M. Rajasekhar Babu enlightened the students on Fundamentals of Multicore Architectures. He explained multiprocessing in a single physical package. Designers may couple cores in a multi-core device tightly or loosely. For example, cores may or may not share caches, and implement message passing or shared-memory inter-core thev mav communication methods. Common network topologies to interconnect include bus, ring, two-dimensional mesh, and crossbar. cores Homogeneous multi-core systems include only identical cores; heterogeneous multi-core systems have cores that are not identical. Just as with single-processor systems, cores in multi-core systems may implement architectures such as VLIW, superscalar, vector, or multithreading.



Dr. M. Rajasekhar Babu delivering the lecture.



Students listening to the lecture.