SREE VIDYANIKETHAN ENGINEERING COLLEGE
(Autonomous)
Sree Sainath Nagar, A. Rangampet-517 102

Department of Electronics and communication Engineering

Lesson Plan

Name of the Subject: ASIC DESIGN (14MT25706)
Class & Semester: M. Tech. (VLSI) – I Semester
Name of the faculty Member: M.BHARATHI

S. No.	Topic	No. of periods	Book(s) followed	Topics for self study
	UNIT – I:			
1.	**ASIC Design Styles:** Introduction	1	T1	ASIC Design flow, ASIC cell libraries.
2.	ASIC Categories	1	T1	
3.	Gate arrays	1	T1	
4.	Standard cells - Cell based ASICs , Mixed mode and analogue ASICs	1	T1	
5.	PLDs	1	T1	
6.	**ASICs – Programmable logic devices**: Overview, PAL – based PLDs	1	T1	
7.	Structures	1	T1	
8.	PAL Characteristics	1	T1	
9.	FPGAs: Intoduction	1	T1	
10.	Selected families	1	T1	
11.	Design outline	1	T1	
	Total periods required:	**11**		
	UNIT – II:			
12.	**ASICs – Design issues:** Design methodologies and design tools	2	T1	Scan test, BIST(Built in self test)
13.	Design for testability	2	T1	
14.	Economies	2	T1	
15.	**ASICs Characteristics and Performance:** Design styles	2	T1	

16.	Gate arrays	1	T1	
17.	Standard cell – based ASICs	1	T1	
18.	Mixed mode and analogue ASICs	1	T1	
	Total periods required:	**11**		
	UNIT -III: ASICS-DESIGN TECHNIQUES			
19.	Overview	1	T1	EDIF(Electronic design interchange format), Design tools- ACTEL,LATTICE.
20.	Design flow and methodology	1	T1	
21.	Hardware description languages	2	T1	
22.	simulation	1	T1	
23.	checking-commercial design tools	1	T1	
24.	FPGA Design tools: XILINX, ALTERA	2	T1	
	Total periods required:	**08**		
	UNIT -IV:			
25.	**LOGIC SYNTHESIS, SIMULATION AND TESTING :** Verilog and logic synthesis	1	T1	FSM synthesis, Memory Synthesis.
26.	VHDL and logic synthesis	1	T1	
27.	Types of simulation	2	T1	
28.	Boundary scan test	1	T1	
29.	Fault simulation	1	T1	
30.	Automatic test pattern generation.	1	T1	
31.	**ASIC Construction:** Floor planning	2	T1	
32.	Placement	2	T1	
33.	Routing	1	T1	
34.	System partition	1	T1	
	Total periods required:	**13**		
	UNIT -V: FPGA PARTITIONING			
35.	Partitioning Methods	2	T1	Information format, **Research Topics:** Application Specific instruction -set processors(ASIPs)
36.	Floor Planning	1	T1	
37.	Placement	1	T1	
38.	Physical Design Flow	1	T1	

39.	Global Routing	1	T1	
40.	Detailed Routing	1	T1	
41.	Special Routing	1	T1	
42.	Circuit Extraction	1	T1	
43.	DRC	1	T1	
Total periods required:		**10**		
Grand total periods required:		**53**		

TEXT BOOKS:

T1: L.J.Herbst, "Integrated circuit engineering", OXFORD SCIENCE Publications, 1996.

REFERENCE BOOKS:

R1: M.J.S.Smith, "Application - Specific integrated circuits", Addison-Wesley Longman Inc 1997.

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Lesson Plan

Name of the Subject: CO-DESIGN (14MT25707)

Name(s) of the faculty Member(s)framing syllabus: P. Madhu Kumar

Class & Semester: M. Tech (VLSI) II SEM. Elective-II

S. No.	Topic	No. of periods	Book(s) followed	Topics for Self Study
	Unit I			
1.	**CO- Design Issues:** Co-design Models	2	T1	Elevator controller in FSM, FSMD models
2.	Architectures	2	T1	
3.	Languages	2	T1	
4.	Generic Co-design Methodology	2	T1	
5.	**Co-Synthesis Algorithms:** Architectural Models	2	T1	
6.	Hardware/Software Partitioning	2	T1	
7.	Distributed System Co-Synthesis	1	T1	
	Total periods required:	**13**		
	Unit II			
8.	**Prototyping and Emulation:** Prototyping and emulation techniques	2	T1	FPGA, ASIC mapping

9.	prototyping and emulation environments	2	T1	
10.	future developments in emulation and prototyping	1	T1	
11.	**Target Architectures- I:** Architecture Specialization techniques	2	T1	
12.	System Communication infrastructure	1	T1	
	Total periods required:	**08**		
	Unit III			
13.	**Target Architectures- II:** Target Architecture and Application System classes	1	T1	ARM and SHARC Architect-ures
14.	Architecture for control dominated systems-8051	2	T1	
15.	Architectures for High performance control	1	T1	
16.	Architecture for Data dominated systems-ADSP21060	1	T1	
17.	TMS320C	1	T1	
18.	Mixed Systems and Less Specialized Systems	1	T1	
	Total periods required:	**07**		
	Unit IV			
19.	**Compilation Techniques and Tools for Embedded Processor Architectures:** Modern embedded architectures	1	T1	Recent Trends in Compiler Design and Development.
20.	embedded software development needs	1	T1	
21.	compilation technologies	2	T1	
22.	Practical consideration in a compiler development environment	1	T1	
23.	**Design Specification and Verification:** Design	1	T1	
24.	co-design	1	T1	
25.	the co-design computational model	1	T1	

26.	concurrency	1	T1	
27.	coordinating concurrent computations	2	T1	
28.	interfacing components	1	T1	
29.	Design verification and implementation verification	1	T1	
30.	verification tools and interface verification	1	T1	
	Total periods required:	**14**		
	Unit V			
31.	**Languages for System- level Specification and Design:** System Level Specification	1	T1	Multi language design examples **Research Topics:** Co-Design of Data dominated embedded systems
32.	Design Representation for System Level Synthesis	2	T1	
33.	System Level Specification Languages	1	T1	
34.	Heterogeneous Specifications and Multi Language Co simulation- Concepts for Multi-language design	1	T1	
35.	Co-simulation models	1	T1	
36.	**Cosyma system**: Overview	1	T1	
37.	Architecture- design flow and user interaction	2	T1	
38.	Partitioning	1	T1	
39.	Synthesis	1	T1	
40.	**Lycos System:** Introduction	1	T1	
41.	Partitioning and Design Space Exploration	1	T1	
	Total periods required:	**13**		
	Grand total periods required:	**55**		

Text Books:

T1: Jorgen Staunstrup, Wayne Wolf, “Hardware / software co- design Principles and Practice”, Springer, 2009.

Reference Books:

R1: Felice Balarine, “Hardware-Software Co-Design of Embedded Systems: The Polis approach”, Springer, 1991.

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Department of Electronics and communication Engineering

Lesson Plan

Name of the Subject: DSP Processors (14MT25708)
Class & Semester: M. Tech. (VLSI) – II Semester
Name of the faculty Member:

S. No.	Topic	No. of periods	Book(s) followed	Topics for self study
UNIT – I: Introduction to Digital Signal Processing				
1.	Introduction, A Digital signal-processing system, The sampling process	1	T1	Design Examples of DFT and FFT.
2.	Discrete time sequences	1	T1	
3.	Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT)	2	T1	
4.	Linear time-invariant systems	1	T1	
5.	Digital filters	1	T1	
6.	Decimation and interpolation	1	T1	
7.	Computational Accuracy in DSP Implementations - Number formats for signals and coefficients in DSP systems	2	T1	
8.	Dynamic Range and Precision	1	T1	
9.	Sources of error in DSP implementations	1	T1	
10.	A/D Conversion errors	1	T1	
11.	DSP Computational errors	1	T1	
12.	D/A Conversion Errors	1	T1	
13.	Compensating filter	1	T1	
Total periods required:		**15**		
UNIT – II: Architectures for Programmable DSP Devices				
14.	Basic Architectural features, DSP Computational Building Blocks	1	T1	Limitations of DSP Processors.
15.	Bus Architecture and Memory	1	T1	
16.	Data Addressing Capabilities	1	T1	
17.	Address Generation Unit	1	T1	
18.	Programmability and Program Execution	2	T1	
19.	Speed Issues	1	T1	
20.	Features for External interfacing	1	T1	
Total periods required:		**08**		
UNIT -III: Programmable Digital Signal Processors				
21.	Commercial Digital signal processing Devices	1	T1	Comparison of TMS320C54XX DSP Processor with other
22.	Data Addressing modes of	2	T1	

	TMS320C54XX DSP Processors			DSP Processors.
23.	Memory space of TMS320C54XX Processors	1	T1	
24.	Program Control	1	T1	
25.	TMS320C54XX instructions and Programming	2	T1	
26.	On-Chip Peripherals	1	T1	
27.	Interrupts of TMS320C54XX processors	1	T1	
28.	Pipeline Operation of TMS320C54XX Processors	1	T1	
Total periods required:		**10**		
UNIT -IV: Analog Devices Family of DSP Devices				
29.	Analog Devices Family of DSP Devices – ALU and MAC block diagram	2	T2	Embedded Digital Signal Processor Design.
30.	Shifter Instruction	1	T2	
31.	Base Architecture of ADSP 2100	1	T2	
32.	ADSP-2181 high performance Processor	1	T2	
33.	Introduction to Blackfin Processor - The Blackfin Processor	1	T3	
34.	Introduction to Micro Signal Architecture	1	T3	
35.	Overview of Hardware Processing Units and Register files	1	T3	
36.	Address Arithmetic Unit, Control Unit	1	T3	
37.	Bus Architecture and Memory, Basic Peripherals	2	T3	
Total periods required:		**11**		
UNIT-V: Interfacing Memory and I/O Peripherals to Programmable DSP Devices				
38.	Memory space organization	1	T1	Applications of DSP Processors. **Research topics:** Cordic Processors
39.	External bus interfacing signals	1	T1	
40.	Memory interface	1	T1	
41.	Parallel I/O interface	1	T1	
42.	Programmed I/O	1	T1	
43.	Interrupts and I/O	1	T1	
44.	Direct memory access (DMA)	1	T1	
Total periods required:		**07**		
Grand total periods required:		**51**		

TEXT BOOKS:

1. Avtar Singh and S. Srinivasan, “Digital Signal Processing”, Thomson Publications, 2004.

2. K Padmanabhan, R.Vijayarajeswaran, Ananthi. S, “A Practical Approach To Digital Signal Processing”, New Age International, 2006/2009.

3. Woon-Seng Gan, Sen M. Kuo, “Embedded Signal Processing with the Micro Signal Architecture”, Wiley-IEEE Press, 2007.

REFERENCE BOOKS:

1. B. Venkataramani and M. Bhaskar, “Digital Signal Processors, Architecture, Programming and Applications”, TMH, 2002.

2. Jonatham Stein, “Digital Signal Processing” , John Wiley, 2005.

3. Lapsley et al, “DSP Processor Fundamentals, Architectures & Features”, S. Chand & Co, 2000.

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Department of Electronics and Communication Engineering

Lesson Plan cum Diary 2013-'14

Name of the Subject: Low power VLSI Design (10MT25702)
Name of the faculty Member: M.Bharathi
Class & Semester: M. Tech (VLSI) II Semester

S. No.	Topic	No. of periods required	Date(s) covered	No. of periods used	Book(s) followed	Remarks
Unit-I						
1.	**Low power Design, An overview:** Introduction to Low-Voltage Low Power Design	2			T1	Comparison of CMOS,SOI and BiCMOS Processes.
2.	Limitations	2			T1	
3.	Silicon-on-Insulator	1			T1	
4.	**MOS/Bi-CMOS PROCESSES:** Bi-CMOS processes	1			T1	
5.	Integration and Isolation considerations	2			T1	
6.	Integrated Analog/Digital CMOS Process	2			T1	
7.	Realization of Bi-CMOS processes	2			T1	
	Total of periods required:	**12**	**Total of periods used:**			
Unit-II: LOW-VOLTAGE/LOW POWER CMOS/ BICMOS PROCESSES						
8.	Deep submicron processes	2			T1	Deep Ultra Submicron Processes.
9.	SOI CMOS	3			T1	
10.	Lateral BJT on SOI	2			T1	
11.	Future trends and directions of CMOS/Bi-CMOS processes	2			T1	
	Total of periods required:	**09**	**Total of periods used:**			
Unit-III: DEVICE BEHAVIOR AND MODELING						
12.	Advanced MOSFET models	2			T1	Comparison of different MOSFET and BJT Models.
13.	Limitations of MOSFET models	2			T1	
14.	Bipolar models	2			T1	
15.	Analytical and Experimental characterization of sub-half micron MOS devices	3			T1	
16.	MOSFET in a Hybrid mode environnent	2			T1	
	Total of periods required:	**11**	**Total of periods used:**			
Unit-IV:						

17.	**CMOS AND Bi-CMOS LOGIC GATES:** Conventional CMOS and Bi-CMOS logic gates	3			T1	Design of Inverter and Buffer using advanced BiCMOS Circuit Techniques.
18.	Performance Evaluation	2			T1	
19.	**LOW- VOLTAGE LOW POWER LOGIC CIRCUITS:** Comparison of advanced Bi-CMOS Digital circuits	2			T1	
20.	ESD-free Bi-CMOS	2			T1	
21.	Digital circuit operation and comparative Evaluation	2			T1	
Total of periods required:		**11**	**Total of periods used:**			
UNIT V:						
22.	**LOW POWER LATCHES AND FLIP FLOPS:** Evolution of Latches and Flip flops	2			T1	Low Power DRAM Design **Research Topic:** Low power clock tree design for Pre-Bond Testing of 3-D Stacked ICs.
23.	Quality measures for latches and Flip flops	2			T1	
24.	Design perspective	2			T1	
25.	**SPECIAL TECHNIQUES** Power Reduction in Clock Networks	1			T1,T2	
26.	CMOS Floating Node	1			T1,T2	
27.	Low Power Bus	1			T1,T2	
28.	Delay Balancing	1			T1	
29	Low Power Techniques for SRAM	1			T1	
Total of periods required:		**11**	**Total of periods used:**			
Grand total of periods required:		**54**	**Grand total of periods used:**			

TEXT BOOKS:

1. Yeo Rofail/ Gohl (3 Authors), "CMOS/Bi-CMOS ULSI low voltage, low power", Pearson Education Asia 1st Indian reprint, 2002.
2. Gary K. Yeap, "Practical Low Power Digital VLSI Design", KAP, 2002.

REFERENCES:

1. Douglas A.Pucknell & Kamran Eshraghian, "Basic VLSI Design", PHI, 3rd edition.
2. J.Rabaey, "Digital Integrated circuits", PH. N.J 1996.

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Department of Electronics and communication Engineering

Lesson Plan

Name of the Subject: Mixed Signal Design (14MT25703)
Class & Semester: M. Tech. (VLSI) – II Semester
Name of the faculty Member: K. Neelima

S. No.	Topic	No. of periods	Book(s) followed	Topics for self study
UNIT – I: SWITCHED CAPACITOR CIRCUITS				
1.	Introduction to Switched Capacitor circuits- basic building blocks	2	T2	Nonlinearity and Mismatch.
2.	Operation and Analysis	3	T2	
3.	Non-ideal effects in switched capacitor circuits	3	T2	
4.	Switched capacitor integrators first order filters	2	T2	
5.	Switch sharing	2	T2	
6.	Biquad filters	2	T3	
Total periods required:		**14**		
UNIT-II: PHASED LOCK LOOP (PLL)				
7.	Basic PLL topology	1	T1	Phase Detector
8.	Dynamics of simple PLL	1	T1	
9.	Charge pump PLLs-Lock acquisition	1	T1	
10.	Phase/Frequency detector and charge pump	1	T1	
11.	Basic charge pump PLL	1	T1	
12.	Non-ideal effects in PLLs-PFD/CP non-idealities	1	T1	
13.	Jitter in PLLs	1	T1	
14.	Delay locked loops, applications	1	T1	
Total periods required:		**08**		
UNIT-III: DATA CONVERTER FUNDAMENTALS				
15.	DC and dynamic specifications	2	T3	Signed Codes, Performance Limitations
16.	Quantization noise	2	T3	
17.	Nyquist rate D/A converters- Decoder based Converters	2	T3	
18.	Binary-Scaled converters	2	T3	
19.	Thermometer-code converters	2	T3	
20.	Hybrid converters	2	T3	
Total periods required:		**12**		
UNIT IV: NYQUIST RATE A/D CONVERTERS				
21.	Successive approximation converters	1	T3	Classification of Data Converters,
22.	Flash converter	1	T3	

23.	Two-step A/D converters	1	T3	Algorithmic (or Cyclic) A/D Converters
24.	Interpolating A/D Converters	1	T3	
25.	Folding A/D converters	1	T3	
26.	Pipelined A/D converters	1	T3	
27.	Time-Interleaved Converters	2	T3	
	Total periods required:	**08**		
	UNIT V: OVERSAMPLING CONVERTERS			
28.	Noise shaping modulators	1	T3	System architectures **Research Topics:** High-speed Wireline, optical and wireless Analog RF front-end circuits
29.	Decimating filters and interpolating filters	1	T3	
30.	Higher order modulators	3	T3	
31.	Delta sigma modulators with multibit quantizers	3	T3	
32.	Delta sigma D/A	1	T3	
	Total periods required:	**09**		
	Grand Total periods required:	**51**		

TEXT BOOKS:

T1: Behzad Razavi, "Design of Analog CMOS Integrated Circuits", TMH Edition, 2002.

T2: Philip E. Allen and Douglas R. Holberg, "CMOS Analog Circuit Design", Oxford University Press, International 2nd Edition/Indian Edition, 2010.

T3: David A. Johns,Ken Martin, "Analog Integrated Circuit Design", Wiley Student Edition, 2013.

REFERENCE BOOKS:

R1: Rudy Van De Plassche, "CMOS Integrated Analog-to-Digital and Digital-to-Analog converters", Kluwer Academic Publishers, 2003.

R2: Richard Schreier, "Understanding Delta-Sigma Data converters", Wiley Interscience, 2005.

R3: R. Jacob Baker, "CMOS Mixed-Signal Circuit Design", Wiley Interscience, 2009.

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Department of Electronics and communication Engineering

Lesson Plan

Name of the Subject: Physical Design Automation **(**14MT25701)
Class & Semester: M. Tech. (VLSI) – II Semester
Name of the faculty Member: Mr.G.Naresh

S. No.	Topic	No. of periods	Book(s) followed	Topics for self study
	UNIT- I INTRODUCTION TO VLSI DESIGN METHODOLOGIES			
1.	Introduction to VLSI Design automation tools	2	T1	VLSI Design problems, structural and logic domain Transistor level design
2.	Introduction to algorithmic graph theory	2	T1	
3.	Computational Complexity	2	T1	
4.	Tractable and Intractable problems	2	T1	
5.	Combinational optimization	2	T1	
	Total periods required:	**10**		
	UNIT- II LAYOUT COMPACTION			
6.	Design rules	2	T1	Symbolic layout Circuit representations
7.	problem formulation	2	T1	
8.	algorithms for constraint graph compaction	2	T1	
9.	placement & partitioning algorithms	2	T1	
10.	Floor planning concepts- shape functions and floor plan sizing	2	T1	
11.	types of routing problems	2	T1	
	Total periods required:	**12**		
	UNIT -III: SIMULATION AND SYNTHESIS			
12.	Gate Level Modeling and Simulation	2	T1	General remarks on VLSI simulation and synthesis
13.	Switch Level Modeling and Simulation	2	T1	
14.	Basic issues and Terminology	2	T1	
15.	Binary-Decision diagrams	2	T1	
16.	Two-Level logic Synthesis	2	T1	
	Total periods required:	**10**		
	UNIT – IV: HIGH LEVEL SYNTHESIS			
17.	Hardware modeling	2	T1	
18.	internal representation of the input algorithm	2	T1	
19.	allocation, assignment and scheduling algorithms	2	T1	

20.	ASAP scheduling	1	T1	
21.	Mobility based scheduling	1	T1	
22.	list scheduling & force-directed scheduling	2	T1	
	Total periods required:	**10**		
UNIT – V: PHYSICAL DESIGN AUTOMATION OF FPGA's & MCM's				
23.	FPGA technologies	1	T2	**Research Topics:** Parallelized EDA applications to fully leverage multi-core machines
24.	Physical Design cycle for FPGA's	1	T2	
25.	Partitioning and Routing for segmented and staggered Models	2	T2	
26.	MCM technologies	1	T2	
27.	MCM physical design cycle	1	T2	
28.	Partitioning	1	T2	
29.	Placement- Chip Array based and Full Custom Approaches	2	T2	
30.	Routing- Maze routing, Multiple stage routing,	2	T2	
31.	Routing and Programmable MCM's	1	T2	
	Total periods required:	**12**		
	Grand total periods required:			

TEXTBOOKS:

T1. S.H.Gerez, "Algorithms for VLSI Design Automation", John wiley & Sons Pvt. Ltd, 2nd edition 1999.

T2. Naveed Sherwani, "Algorithms for VLSI Physical Design Automation", Springer International Edition, 3rd edition, 2005.

REFERENCES:

R1. Hill & Peterson, "Computer Aided Logical Design with Emphasis on VLSI", John wiley & Sons Pvt. Ltd,4th edition, 1993.

R2. Wayne Wolf, "Modern VLSI Design Systems on silicon", Pearson Education Asia, 2nd Edition, 1998

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Department of Electronics and communication Engineering

Lesson Plan

Name of the Subject: RFIC DESIGN (14MT25704)
Class & Semester: M. Tech. (VLSI) – II Semester
Name of the faculty Member:

S. No.	Topic	No. of periods	Book(s) followed	Topics for self study
UNIT – I: BASIC CONCEPTS IN RF DESIGN				
1.	Introduction to RF Design	1	T1	BJT and MOSFET behavior at RF frequencies, Modeling of the transistors and SPICE models, Passive Devices
2.	Units in RF design	1	T1	
3.	Time Variance and Nonlinearity			
4.	Effects of nonlinearity	1	T1	
5.	random processes and Noise	1	T1	
6.	Definitions of sensitivity and dynamic range	1	T1	
7.	Passive impedance transformation	1		
8.	Scattering parameters	1	T1	
Total periods required:		**07**		
UNIT – II: TRANSCEIVER ARCHITECTURES				
9.	General considerations	1	T1	Analog and digital Modulations, Multiple Access Techniques, Wireless standards
10.	Heterodyne receivers	2	T1	
11.	Modern heterodyne receivers	1	T1	
12.	Direct conversion receivers	2	T1	
13.	Image-Reject receivers	2	T1	
14.	Low-IF receivers	2	T1	
15.	Direct Conversion transmitters	2	T1	
16.	Modern direct conversion Transmitters	1	T1	
17.	Heterodyne Transmitters, Other Transmitter Architectures	1	T1	
Total periods required:		**14**		
UNIT -III: LNA AND MIXERS				
18.	General considerations	1	T1	High IP_2 LNAs, Nonlinearity calculations, Improved mixer topologies
19.	Problem of input matching	1	T1	
20.	Low Noise Amplifiers design in various topologies	2	T1	
21.	Gain Switching	1	T1	
22.	Band Switching		T1	
23.	Mixers-General considerations	1	T1	

24.	Passive down conversion mixers	2	T1	
25.	Active down conversion mixers	2	T1	
26.	Up conversion mixers	1	T1	
Total periods required:		**11**		
UNIT – IV: OSCILLATORS				
27.	Performance parameters	1	T1	Quadrature Oscillators
28.	Basic principles	1	T1	
29.	Cross coupled oscillator	1	T1	
30.	Three point oscillators	1	T1	
31.	Voltage Controlled Oscillators	2	T1	
32.	LC VCOs with wide tuning range	2	T1	
33.	phase noise	1	T1	
34.	Mathematical model of VCOS	1	T1	
Total periods required:		**10**		
UNIT – V: PLL AND POWER AMPLIFIER				
35.	Phase detector	1	T1	Frequency Synthesizes
36.	Type-I PLLs	1	T1	
37.	Type-II PLLs	1	T1	
38.	PFD/CP Nonidealities	1	T1	
39.	Phase noise in PLLs	1	T1	**Research Topics:** RF Front End Design For Cognitive Radio, Ultra Low Power RFIC Design for Wireless communication
40.	Loop Bandwidth			
41.	Power Amplifiers-General considerations	1	T1	
42.	Classification of power amplifiers	2	T1	
43.	High- Efficiency power amplifiers	2	T1	
44.	Cascode output stages	1	T1	
45.	Large signal impedance matching	1	T1	
46.	Linearization techniques	1	T1	
Total periods required:		**13**		
Grand total periods required:		**55**		

Text Books:

T1: B.Razavi, “RF Microelectronics”, Prentice-Hall, 2nd edition, 1998.

Reference Books:

R1: T.H.Lee, “The Design of CMOS Radio-Frequency Integrated Circuits", Cambridge University Press, 2nd , 1998.

R2: R.Jacob Baker, Harry W.Li, D.E. Boyce, “CMOS Circuit Design, Layout and Simulation”, Prentice-Hall of India, 1998.

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SREE VIDYANIKETHAN ENGINEERING COLLEGE

(Autonomous)

Sree Sainath Nagar, A. Rangampet-517 102

Department of Electronics and communication Engineering

Lesson Plan

Name of the Subject: Transform Techniques (14MT13808)
Class & Semester: M. Tech. (CMS & DECS) – I Semester
Name of the faculty Member: Mr. K. V Koteswara Rao

S. No.	Topic	No. of periods	Book(s) followed	Topics for self study
UNIT – I				
1.	**Review of Transforms**: Vector space, functions and function spaces	1	T2	Parseval's Identity for the CWT, Inverse CWT as a many-to-One Operation.
2.	Fourier transform	2	T2	
3.	Short-Time Fourier Transform	2	T2	
4.	Walsh, Hadamard, Haar	1	R1	
5.	Slant, KLT, Hilbert transforms	1	R1	
6.	**Continuous Wavelet Transform:** Introduction, Continuous-Time Wavelets	1	T1	
7.	Definition of the CWT	1	T1	
8.	The CWT as a correlation	1	T1	
9.	Constant Q-Factor Filtering Interpretation and Time-Frequency Resolution	2	T1	
10.	The CWT as an operator	1	T1	
11.	Inverse CWT	1	T1	
Total periods required:		**14**		
UNIT -II: DISCRETE WAVELET TRANSFORM AND ORTHOGONAL WAVELET DECOMPOSITION				
12.	Introduction	1	T1	Regularity and convergence, Band limited Bi-orthogonal Decomposition, Design and Selection of Wavelets.
13.	Approximations of vectors in nested linear vector spaces	1	T1	
14.	Example of an MRA-Bases for the Approximation Subspaces and Harr Scaling Function	2	T1	
15.	Bases for the Detail Subspaces and Harr Wavelet	2	T1	
16.	Digital Filter Implementation of the Harr Wavelet Decomposition	2	T1	
Total periods required:		**08**		
UNIT -III: MRA ORTHONORMAL WAVELETS, AND THEIR RELATIONSHIP TO FILTER BANKS				
17.	Introduction	1	T1	Daubechies construction of Orthonormal Scaling
18.	Formal Definition of an MRA	1	T1	
19.	Construction of a General Orthonormal	2	T1	

	MRA			Functions.
20.	A Wavelet basis for MRA	2	T1	
21.	Digital Filtering Interpretation	1	T1	
22.	Examples of Orthogonal Basis Generating Wavelets	1	T1	
23.	Interpreting Orthonormal MRAs for Discrete time signals	2	T1	
24.	Miscellaneous issues Related to PRQMF Filter Banks	1	T1	
25.	Generating Scaling Functions and Wavelets from Filter Coefficients	1	T1	
Total periods required:		**12**		
UNIT – IV: ALTERNATIVE WAVELET REPRESENTATIONS				
26.	Bi-orthogonal Wavelet Bases	2	T1	M-Band Wavelets, Lifting Scheme.
27.	Filtering Relationship for Bi-orthogonal Filters	1	T1	
28.	Examples of Bi-orthogonal Scaling Functions and Wavelets	1	T1	
29.	Two-Dimensional Wavelets	2	T1	
30.	Non-separable Multidimensional Wavelets	1	T1	
31.	Wavelet Packets	2	T1	
Total periods required:		**09**		
UNIT – V: APPLICATIONS OF WAVELETS				
32.	Wavelet De-noising	2	T1	Wavelets in Boundary Value Problems. **Research Topics:** Adaptive Wavelet Transforms, Stationary Wavelet Transforms, Cycle Wavelet Transforms.
33.	Speckle Removal	1	T1	
34.	Edge Detection and Object Isolation	2	T1	
35.	Image Fusion	2	T1	
36.	Object Detection by Wavelet Transforms of Projections	1	T1	
37.	Scaling Functions as signaling pulses	2	T1	
38.	Discrete Wavelet Multitone Modulation	1	T1	
Total periods required:		**11**		
Grand total periods required:		**54**		

Text Books:

T1: Raghuveer M.Rao and Ajit S.Bopardikar, "*Wavelet Transforms-Introduction to theory and applications*", Pearson edu, 1998.

T2: Soman.K.P, Ramachandran.K.I, Resmi.N.G, "*Insight into Wavelets from theory to Practice"*, PHI, Third Edition, 2010.

Reference Books:

R1. R. C. Gonzalez, R. E. Woods, "*Digital Image Processing*," 2nd Edition, Pearson Education, 1992.

R2: Jaideva C Goswami, Andrew K.Chan, "*Fundamentals of Wavelets-Theory, Algorithms and Applications"*, John Wiley and sons, 1999.

R3: C.Sidney Burrus, Ramesh A Gopinath and Haitao Guo, "*Introduction to Wavelets and Wavelet Transforms"*, Prentice Hall, 1998.

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Department of Electronics and communication Engineering

Lesson Plan

Name of the Subject: Wireless Sensor Networks (14MT257709)
Class & Semester: M. Tech. (CMS) – II Semester
Name of the faculty Member: Dr. V. R. Anitha

S. No.	Topic	No. of periods	Book(s) followed	Topics for self study
UNIT – I: INTRODUCTION TO WIRELESS SENSOR NETWORKS				
1.	Challenges for wireless sensor networks	1	T1	Security in Sensor networks
2.	Comparison of sensor network with ad hoc network	1	T1	
3.	Single node architecture - Hardware components	2	T1	
4.				
5.	Energy consumption of sensor nodes	2	T1	
6.				
7.	Network architecture: Sensor network scenarios - types of sources and sinks	1	T1	
8.	Single hop versus multi-hop networks, multiple sinks and sources	1	T1	
9.	Design principles for wireless sensor networks	3	T1	
10.				
11.				
Total periods required:		**11**		
UNIT – II: PHYSICAL LAYER				
12.	Introduction, wireless channel and communication fundamentals	1	T1	Localization, IEEE 802.15.4 low rate WPAN
13.	Frequency allocation	1	T1	
14.	Modulation and demodulation	1	T1	
15.	Wave propagation effects and noise,	1	T1	
16.	Channels models	1	T1	
17.	Spread spectrum communication	1	T1	
18.	Packet transmission and synchronization	1	T1	
19.	Quality of wireless channels and measures for improvement	1	T1	
20.	Physical layer and transceiver design consideration in wireless sensor networks - Energy usage profile	1	T1	
21.	Choice of modulation, Power Management .	2	T1	
22.				
Total periods required:		**11**		
UNIT -III: DATA LINK LAYER				
23.	MAC protocols: fundamentals of wireless MAC protocols	2	T1	Practical implementation issues
24.	Requirements and design constraints for wireless MAC protocols			

25.	Important classes of MAC protocols,	1	T1	
26.	MAC protocols for wireless sensor networks	1	T1	
27.	Low duty cycle protocols and wakeup concepts	1	T1	
28.	Sparse topology and energy management (STEM)	1	T1	
29.	S-MAC	1	T1	
30.	Wakeup radio concepts	1	T1	
31.	Contention-based protocols - CSMA protocols	1	T1	
32.	PAMAS	1	T1	
33.	Schedule-based protocols - SMAC, BMAC	1	T1	
34.	Traffic-adaptive medium access protocol (TRAMA)	1	T1	
35.	Link Layer protocols – fundamentals task and requirements	1	T1	
36.	Error control - Causes and characteristics of transmission errors, ARQ techniques,	1	T1	
37.	FEC techniques	1	T1	
38.	Hybrid schemes, Power control	1	T1	
Total periods required:		**16**		
UNIT – IV: NETWORK LAYER				
39.	Gossiping and agent-based uni-cast forwarding - Basic idea, Randomized forwarding, Energy-efficient unicast	1	T1	
40.	Broadcast and multicast - Source-based tree protocols	1	T1	
41.	Shared, core-based tree protocols, Mesh-based protocols	1	T1	
42.	Geographic routing - Basics of position-based routing	1	T1	
43.	Geocasting	1	T1	
44.	Mobile nodes - Mobile sinks, Mobile data collectors	1	T1	
45.	Mobile regions	1	T1	
46.	Data centric and content-based networking - Introduction	1	T1	
47.	Data-centric routing	1	T1	
48.	Data aggregation	1	T1	
Total periods required:		**10**		
UNIT – V: TRANSPORT LAYER				
49.	The transport layer and QoS in wireless sensor networks - Quality of service/reliabilitym, Transport protocols	1	T1	Sensor Node Hardware- Node-level software platforms **standardization:** IEEE 802.15.4 & IEEE 802.11 **Research Topics:** Node-level simulators Wireless Sensor
50.	Coverage and deployment - Sensing models, Coverage measures	1	T1	
51.	Uniform random deployments: Poisson point processes, Coverage of random deployments: Boolean sensing model, general sensing model	2	T1	

52.	Coverage determination, Coverage of grid deployments, Reliable data transport	1	T1 T1	Networks
53.	Single packet delivery - Using a single path, Multiple paths, Multiple receivers	1	T1	
54.	Congestion control and rate control - Congestion situations in sensor networks	1	T1	
55.	Mechanisms for congestion detection and handling	1		
56.	Protocols with rate control	1		
57.	The CODA congestion-control framework	1		
Total periods required:		**09**		
Grand total periods required:		**57**		

Text Books:

T1: Holger Karl , Andreas willig “Protocol and Architecture for Wireless Sensor Networks”, John wiley publication, Oct 2007.

Reference Books:

R1: Feng zhao, Leonidas guibas, Elsivier , “Wireless Sensor Networks: an information processing approach –publication, 2004.

R2: Edgar H .Callaway, First Edition,”Wireless Sensor Networks : Architecture and protocol”, CRC press 2003.

R3: C.S.Raghavendra Krishna, M.Sivalingam and Tarib znati, “Wireless Sensor Networks”, Springer publication, 2006

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