SREE VIDYANIKETHAN ENGINEERING COLLEGE

(Autonomous)

Sree Sainath Nagar, A. Rangampet-517 102

Department of Electronics and communication Engineering

Lesson Plan

Name of the Subject: Advanced Digital Signal Processing, (14MT15706)

Class & Semester: M. Tech.– I Semester, VLSI (Elective-I) & CMS

Name of the faculty Member: Ms D Leela Rani

S. No.	Topic	No. of periods	Book(s) followed	Topics for self study
	UNIT – I: MULTIRATE FILTER BANKS			
1.	Decimation	1	T1	Discrete Wavelet Transform
2.	Interpolation	1	T1	
3.	Sampling rate conversion by a rational factor I/D	1	T1	
4.	Multistage Implementation of sampling rate conversion.	1	T1	
5.	**Digital Filter Banks**: Two-Channel Quadrature-Mirror Filter Bank,	1	T1	
6.	Elimination of aliasing, condition for Perfect Reconstruction,	2	T1	
7.	Polyphase form of QMF bank,	2	T1	
8.	Linear phase FIR QMF bank, IIR QMF bank ,	1	T1	
9.	Perfect Reconstruction Two-Channel FIR QMF Bank	2	T1	
	Total periods required:	**12**		
	UNIT II: NON-PARAMETRIC METHODS OF POWER SPECTRAL ESTIMATION			
10.	Estimation of spectra from finite duration observation of signals	2	T1	Correlation, Power Spectrum and its properties
11.	**Non-Parametric Methods**: Bartlett, Welch methods.	2	T1	
12.	Blackmann & Tukey methods.	2	T1	
13.	Performance Characteristics of Nonparametric Power Spectrum Estimators	2	T1	
14.	Computational Requirements of Nonparametric Power Spectrum Estimates	2	T1	
	Total periods required:	**10**		
	UNIT -III: PARAMETRIC METHODS OF POWER SPECTRAL ESTIMATION			
15.	Autocorrelation & Its Properties	2	T1	Stationary, Non-Stationary &Wide sense stationary processes
16.	Relation between auto correlation and model parameters	2	T1	
17.	Yule-Walker & Burg Methods	2	T1	
18.	MA model for power spectrum estimation	2	T1	
19.	ARMA model for power spectrum estimation	2	T1	
	Total periods required:	**10**		
	UNIT – IV: DSP ALGORITHMS			
20.	Fast DFT algorithms based on Index mapping	2	T2	Composite FFT
21.	Sliding Discrete Fourier Transform	2	T2	
22.	DFT Computation Over a narrow Frequency Band	2	T2	
23.	Split Radix FFT	2	T2	

24.	Linear filtering approach to Computation of DFT using Chirp Z-Transform	2	T2	
	Total periods required:	**12**		
	UNIT – V: APPLICATIONS OF DIGITAL SIGNAL PROCESSING			
25.	Digital cellular mobile telephony	1	R1	Subband coding of speech and audio signals, spectral analysis of random signals. **Research Topics:** Methods to Minimize Finite Word Length Effect, Wavelets in Digital Filter Banks. Multirate signal Processing
26.	Adaptive telephone echo cancellation	1	R1	
27.	High quality A/D conversion for digital Audio	2	R1	
28.	Efficient D/A conversion in compact hi-fi systems	2	R1	
29.	Acquisition of high quality data	1	R1	
30.	Multirate narrow band digital filtering	2	R1	
31.	High resolution narrowband spectral analysis	2	R1	
	Total periods required:	**11**		
	Grand total periods required:	**55**		

TEXT BOOKS:

T1. John G. Proakis, Dimitris G. Manolakis, *Digital signal processing, principles, Algorithms and applications,* Prentice Hall, 4th Edition, 2007.

T2. Sanjit K Mitra, "*Digital signal processing, A computer base approach",* McGraw-Hill Higher Education, 4th Edition, 2011.

REFERENCE BOOKS:

R1. Emmanuel C Ifeacher Barrie. W. Jervis, "*DSP - A Practical Approach*", Pearson Education, 2nd Edition, 2002.

R2. A.V. Oppenheim and R.W. Schaffer, "*Discrete Time Signal Processing",* PHI, 2nd Edition, 2006.

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Department of Electronics and communication Engineering

Lesson Plan

Name of the Subject: Analog IC Design (14MT15701)
Class & Semester: M. Tech. (VLSI) – I Semester
Name of the faculty Member: T. Krishna Murthy

S. No.	Topic	No. of periods	Book(s) followed	Topics for self study
UNIT – I:				
1.	**Basic MOS Device Physics:** General Considerations, MOS I/V Characteristics	2	T1	Second-Order Effects and Choice of Device Models.
2.	Second-Order Effects	1		
3.	MOS Device Models	1	T1	
4.	**Single Stage Amplifiers:** Common-Source Stage	2	T1	
5.	Source follower, Common Gate Stage	2	T1	
6.	Cascode Stage	1	T1	
7.	Differential Amplifiers	3	T1	
8.	Current Mirrors	3	T1	
Total periods required:		**15**		
UNIT- II: Frequency Response and Noise Characteristics Of Amplifiers				
9.	Frequency Response-General Considerations	1	T1	Types of Noise, Representation of Noise in Circuits and Noise Bandwidth.
10.	Common-Source Stage, Source follower	1	T1	
11.	Common Gate Stage, Cascode Stage, Differential pair	2	T1	
12.	Noise- Statistical Characteristics of Noise	1	T1	
13.	Noise in Single Stage Amplifiers, Noise in Differential Pairs.	2	T1	
Total periods required:		**07**		
UNIT- III: Feedback Circuits and Operational Amplifiers				
14.	Feedback Circuits-General considerations	2	T1	Comparison of performance of Various and Common-Mode Feedback.
15.	Feedback Topologies	2	T1	
16.	Effect of Loading, Effect of Feedback on Noise	2	T1	
17.	Operational Amplifiers- General considerations	1	T1	
18.	One-stage Op Amps	1	T1	
19.	Two - stage Op Amps, Gain boosting	2	T1	
20.	Input range limitations, slew rate	1	T1	
21.	Power Supply Rejection, noise in Op Amps	1	T1	
Total periods required:		**12**		
UNIT- IV:				

22.	**Stability and Frequency Compensation:** General considerations, Multipole Systems	1	T1	General Consideration, Case Study in Bandgap References.
23.	Phase Margin, Frequency Compensation, Compensation of Two-Stage Op Amps	2	T1	
24.	Other Compensation Techniques	1	T1	
25.	**Bandgap References:** Supply-Independent Biasing	1	T1	
26.	Temperature-independent References	1	T1	
27.	PTAT Current Generation, Constant - Gm Biasing, Speed and Noise Issues.	2	T1	
Total periods required:		**08**		
UNIT- V: Introduction To Switched–Capacitor Circuits				
28.	General Considerations	1	T1	**Research Topic-** Hybrid Mixed Analog/Digital PLLs, Reconfigurable Phase Arrays, CMOS Cognitive Radio
29.	Sampling Switches	3	T1	
30.	Switched-Capacitor Amplifiers	3	T1	
31.	Switched-Capacitor Integrator, Switched-Capacitors Common-Mode Feedback	2	T1	
Total periods required:		**09**		
Grand Total periods required:		**51**		

TEXT BOOKS:

T1: Behzad Razavi, “Design of Analog CMOS Integrated Circuit”, Tata-McGraw-Hill, 2002.

REFERENCES:

R1: D.A.John & Ken Martin, “Analog Integrated Circuit Design”, John Wiley, 1997.
R2: Philip Allen & Douglas Holberg, “CMOS Analog Circuit Design”, Oxford University Press, 2002.

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Department of Electronics and communication Engineering

Lesson Plan

Name of the Subject: Computational Techniques for Microelectronics (14MT15702)
Class & Semester: M. Tech. (VLSI) – I Semester
Name of the faculty Member: K.NEELIMA

S. No.	Topic	No. of periods	Book(s) followed	Topics for self study
UNIT – I: BASIC COMPUTATION TOOLS				
1.	Linear systems and matrices – matrix formalities	1	T1	Linear and Nonlinear mathematics
2.	condition of matrix systems	1	T1	
3.	Techniques for matrix solution	2	T1	
4.	Mixed boundary condition	2	T1	
5.	Nonlinear Systems – scalar equations	2	T1	
6.	Matrix equations	2		
7.	Approximation, interpolation, curve fitting	2	T1	
8.	Numerical Integration	2	T1	
Total periods required:		**14**		
UNIT – II: COMPUTATIONAL TOOLS FOR APPLICATIONS				
9.	Finite difference techniques	1	T1	Partial Differential Equations
10.	Initial Value problems	2	T1	
11.	Energy Methods and Minimization	2	T1	
12.	Finite Element Methods	2	T1	
13.	Dynamic methods in applied mechanics	2	T1	
Total periods required:		**09**		
UNIT -III: ADVANCED COMPUTATIONAL TOOLS				
14.	Method of characteristics	2	T1	Applications of partial differential equations
15.	Classification of partial Differential equations	2	T1	
16.	Investigations in Engineering	2	T1	
17.	Finite volume methods – Direct Analysis	2	T1	
Total periods required:		**08**		
UNIT -IV: GRID GENERATION AND ERROR ESTIMATES				
18.	Grid generation	2	T2	Multi levels and Domain decomposition
19.	Triangulation	2	T2	
20.	errors and mesh Selection	2	T2	

21.	Refinement Algorithms	2	T2	
22.	Mesh Redistribution	2	T2	
23.	Moving Grids	2	T2	
Total periods required:		**10**		
UNIT -V: APPLICATIONS TO DEVICE AND PROCESS SIMULATION				
24.	Applications to device and process simulation	2	T3	Model Parameters design
25.	Layout algorithms	3	T3	**Research Topics:** Time Series prediction to computational NeuroScience
26.	Yield estimation algorithms	3	T3	
27.	Symbolic analysis and Synthesis of Analog ICs	3	T3	
Total periods required:		**11**		
Grand total periods required:		**52**		

TEXT BOOKS:

T1: Herbert Koenig,"Modern Computational methods", CRC Press, 1988.

T2: Graham F.carey, " Computational Grids: generations, adaptation & Solution Strategies", CRC Press, 1997.

T3: Naveed A. Sherwani,"Algorithms for VLSI Physical Design Automation", Kluwer Academic Publishers, 1993.

REFERENCE BOOKS:

R1: L.Pallage, R.Rohrer And C.Visweswaraiah, "Electronic Circuit and System Simulation Methods", McGraw Hill, 1995.

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Department of Electronics and communication Engineering

Lesson Plan

Name of the Subject: DIGITAL IC DESIGN (14MT15704)
Class & Semester: M. Tech. (VLSI) – I Semester
Name of the faculty Member: Mr. K.V.Rajendra Prasad

S. No.	Topic	No. of periods	Book(s) followed	Topics for self study
UNIT – I: CMOS INVERTERS CHARACTERSTICS and DESIGN STYLES				
1.	Static and Dynamic characteristics	3	R3	CMOS Inverter Operation, Pull-up and Pull Down Networks.
2.	Introduction to Static and Dynamic CMOS design	1	T1	
3.	Domino Logic	1	T1	
4.	NORA logic	1	T1	
5.	Combinational	1	T1	
6.	Sequential circuits	2	T1	
	Total periods required:	**09**		
UNIT – II: LOGICAL EFFORTS AND MEMORY DESIGN				
7.	Methods of Logical Effort for transistor sizing	2	R1	Logical Effort Problems on Complex Combinational Circuits.
8.	Power consumption in CMOS Gates	1	R1	
9.	Low power CMOS design	1	T1	
10.	CMOS Memory design	1	T1	
11.	SRAM design	2	R1	
12.	DRAM design	2	R1	
	Total periods required:	**09**		
UNIT -III: DESIGN METHODOLOGY AND TOOLS				
13.	Introduction	1	T3	
14.	Structured Design Strategies	2	T3	Programmable Logic, Gate Array ,Full Custom Design .
15.	Design Methods	2	T3	
16.	Design Flows	2	T3	
17.	Design Economics	1	T3	
18.	Data Sheets and Documentation	2	T3	
	Total periods required:	**10**		
UNIT – IV: LAYOUT DESIGN RULES				
19.	Need for Design Rules	1	T1	Rising and falling Delays of CMOS Design , Layout Design for
20.	Mead Conway Design Rules for the Silicon Gate NMOS Process	2	T1	
21.	CMOS Based Design Rules	2	T1	

22.	Simple Layout Examples.	1	T1	Complex Logic Circuits.
23.	Sheet Resistance	1	T2	
24.	Area Capacitance	1	T2	
25.	Wire Capacitance	1	T2	
26.	Drive Large Capacitive Load.	2	T2	
Total periods required:		**11**		
UNIT – V: SUBSYSTEM DESIGN PROCESS				
27.	General arrangement of 4-bit Arithmetic Processor	2	T2	Bus Arrangements in Processor Architecture, Adder and Subtractor Design using ALU. **Research Topics:** Low Power Digital IC Design and High Speed Digital IC Design.
28.	Design of 4-bit shifter	1	T2	
29.	Design of ALU sub-system	1	T2	
30.	Implementing ALU functions with an adder	1	T2	
31.	Multipliers	5	T2	
32.	Modified Booth's algorithm.	1	T2	
Total periods required:		**11**		
Grand total periods required:		**50**		

TEXT BOOKS:

T1: Eugene D Fabricus, "Introduction to VLSI Design, "McGraw Hill International Edition, 1990.

T2: Kamran Eshranghian, Douglas A.Puknell and Sholh Eshranghian"Essential of VLSI Circuits and Systems", PHI , 1st edition,2005.

T3: Neil H. E. Weste, David Money Harris,"CMOS VLSI Design-A Circuit and Systems Perspective", Pearson 4th Edition,2011.

REFERENCES:

R1: John P.Uyemura, "Introduction to VLSI Circuits and Systems", Wiley Edition, 2002.

R2: Sung-Mo Kang & Yusuf Leblebici, "CMOS Digital Integrated Circuits - Analysis & Design", McGraw Hill, 2nd edition, 1999.

R3: Jan M Rabaey, "Digital Integrated Circuits-A Design Perspective", Prentice Hall, 1st edition, 1997.

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Department of Electronics and communication Engineering

Lesson Plan

Name of the Subject: Device Modeling (14MT15703)
Class & Semester: M. Tech. (VLSI) – I Semester
Name of the faculty Member: M.BHARATHI

S. No.	Topic	No. of periods	Book(s) followed	Topics for self study
UNIT – I: BASIC DEVICE PHYSICS				
1.	**Two Terminal MOS Structure**: Flat-band voltage	1	T1	**Semiconductors, Junctions and MOSFET overview-** Qualitative Description of MOS transistor Operation, MOS characteristics. Properties of regions of operations,
2.	Potential balance & charge balance	1	T1	
3.	Effect of Gate-substrate voltage on surface condition	2	T1	
4.	Inversion	2	T1	
5.	Small signal capacitance	1	T1	
6.	**Three Terminal MOS Structure:** Contacting the inversion layer	1	T1	
7.	Body effect, Regions of inversion,	3	T1	
8.	Pinch- off voltage	1	T1	
	Total periods required:	**12**		
UNIT – II: FOUR TERMINAL MOS TRANSISTOR				
9.	Transistor regions of operation	1	T1	Source Referenced Vs body referenced modeling, Model Accuracy, Model comparison .
10.	General charge sheet models	2	T1	
11.	Regions of inversion in terms of terminal voltage	1	T1	
12.	strong inversion	2	T1	
13.	weak inversion, moderate inversion	2	T1	
14.	interpolation models	1	T1	
15.	effective mobility	1	T1	
16.	temperature effects	1	T1	
17.	Breakdown , The p-channel MOS FET	1	T1	
18.	enhancement and depletion type	1	T1	
19.	model parameter values	1	T1	
	Total periods required:	**14**		
UNIT -III: MOS TRANSISTOR WITH ION-IMPLANTED CHANNELS & SMALL DIMENSION EFFECTS				

20.	Enhancement of nMOS	3	T1	Channel length modulation Sub threshold regions, Short channel effects
21.	Depletion nMOS	2	T1	
22.	Enhancement pMOS	2	T1	
23.	barrier lowering two dimensional charge sharing and threshold voltage	2	T1	
24.	punch-through	1	T1	
25.	carrier velocity saturation	1	T1	
26.	hot carrier effects	1	T1	
27.	Scaling	1	T1	
28.	effects of surface and drain series resistance	1	T1	
29.	effects due to thin oxides and high doping	1	T1	
	Total periods required:	**14**		
UNIT -IV: MOS TRANSISTOR IN DYNAMIC OPERATION- LARGE SIGNAL MODELING:				
30.	Quasi static operation,	1	T1	Non Quasi static Analysis.
31.	Terminal currents in Quasi static operation,	1	T1	
32.	Evaluation of Charges in Quasi static operation,	2	T1	
33.	Transit time under DC conditions,	1	T1	
34.	Limitations of Quasi static Model,	1	T1	
	Total periods required:	**06**		
UNIT-V:SMALL SIGNAL MODELING FOR LOW, MEDIUM AND HIGH FREQUENCIES:				
35.	low, Medium frequency small signal model for the intrinsic part	2	T1	Noise –White noise, Flicker Noise, Small Dimension Effects, Equivalent Circuit Model, Considerations of MOSFET in RF Applications. **Research Topics:** Research Needs for Compact Modeling, Effect of High Fields on MOS Device and Circuit.
36.	Small signal model for Extrinsic Part	1	T1	
37.	A complete Quasi static Model	2	T1	
38.	Y-Parameter models	1	T1	
39.	Non Quasi static Models	2	T1	
	Total periods required:	**8**		
	Grand total periods required:	**54**		

TEXT BOOKS:

T1 :Y. Tsividis," Operations and Modeling of the MOS Transistor", Oxford university Press,2nd edition.

REFERENCE BOOKS:

R1: Trond Ytterdal, Yuhua Cheng &Tor A. Fjeldly " Device Modeling for Analog and RF CMOS Circuit Design" Wiley Publication ,2003.

R2:Donald A Neamen & Dhrubes Biswas "Semiconductor Physics and Devices" Special Indian Edition ,2012.

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Lesson Plan

Name of the Subject: FPGA Applications (14MT15707)
Class & Semester: M. Tech. (VLSI) – I Semester
Name of the faculty Member: T. Krishna Murthy

S. No.	Topic	No. of periods	Book(s) followed	Topics for self study
UNIT- I:				
1.	**Introduction to Field Programmable Gate Arrays(FPGA):** Evolution of Programmable Devices, What is FPGA, Applications of FPGAs. Programming Technologies in FPGAs.	2	T1	Commercially Available FPGAs , Actel ACT-3, Plus Logic FPGA, QuickLogic FPGA, Algotronix FPGA and Concurrent Logic FPGA,
2.	**Xillinx and Actel FPGAs :** Xilinx FPGAs –XC2000, XC3000 and Xillinx XC4000	2	T1	
3.	Actel FPGAs – Actel ACT-1, Actel ACT-2	1	T1	
4.	Altera FPGAs, Plessey FPGA	2	T1	
5.	Advanced Micro Devices (AMD) FPGA, FPGA Design Flow.	2		
6.	Technology Mapping for FPGAs- Logic Synthesis, Lookup Table Technology Mapping	1		
Total periods required:		**10**		
UNIT- II: FPGA-based Embedded Processor				
7.	Hardware–Software Task Partitioning, FPGA Fabric Immersed Processors.	2	T2	Robot Axis Position Control
8.	Interfacing Memory to the Processor, Interfacing Processor with Peripherals	3	T2	
9.	Design Re-use Using On-chip Bus Interface, Creating a Customized Microcontroller.	2	T2	
Total periods required:		**07**		
UNIT- III: Motor Control using FPGA				
10.	Introduction to Motor Drives, Digital Block Diagram for Robot Axis Control-Position Loop, Speed Loop and Power Module	2	T2	Permanent Magnet Synchronous Motor (PMSM), Test Environment for the Robot Controller and
11.	Case Studies for Motor Control-Stepper Motor Controller	2	T2	

12.	Permanent Magnet DC Motor, Brushless DC Motor	2	T2	FPGA Design Test Methodology
13.	Permanent Magnet Rotor (PMR) Synchronous Motor	2	T2	
14.	Prototyping Using FPGAs	1	T2	
	Total periods required:	**09**		
	UNIT- IV: FIR Digital Filters Using FPGA			
15.	Digital Filters, FIR Filter-FIR Filter with Transposed Structure	2	T3	IP Core FIR Filter Design and Comparison of DA- and RAG-Based FIR Filters.
16.	Symmetry in FIR Filters, Linear-phase FIR Filters	2	T3	
17.	Designing FIR Filters-Direct Window Design Method, Equiripple Design Method	2	T3	
18.	Constant Coefficient FIR Design-Direct FIR Design	2	T3	
19.	FIR Filter with Transposed Structure	3	T3	
20.	FIR Filters Using Distributed Arithmetic	3	T3	
21.	**Total periods required:**	**14**	T3	
22.	**UNIT- V: IIR Digital Filters Using FPGA**			
23.	Introduction to IIR, IIR Digital Filter	2	T3	**Research Topic-** Advanced FPGA design and FPGA design of Software Defined Radios
24.	IIR Coefficient Computation	1	T3	
25.	IIR Filter Implementation	2	T3	
26.	Finite wordlength effects and Optimization of the Filter Gain Factor.	1	T3	
27.	Fast IIR Filter-Time domain Interleaving, Clustered and Scattered Look-Ahead Pipelining	2	T3	
28.	IIR Decimator Design and Parallel Processing	2	T3	
	Total periods required:	**10**		
	Grand total periods required:	**50**		

TEXT BOOKS:

T1. S.Brown, R.Francis, J.Rose, Z.Vransic, "Field Programmable Gate Array", Kluwer Publication, 1992.

T2. Rahul Dubey, "Introduction to Embedded System Design Using Field Programmable Gate Arrays", Springer , 2009.

T3. Uwe Meyer-Baese, "Digital Signal Processing with Field Programmable Gate Arrays", Springer Series, 2007.

REFERENCES:

R1. S.Trimberger, Edr., “Field Programmable Gate Array Technology”, Kluwer Academic Publications, 1994.

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Department of Electronics and communication Engineering

Lesson Plan

Name of the Subject: IC Fabrication (14MT15705)
Class & Semester: M. Tech. (VLSI)
Name of the faculty Member: C Venkata Sudhakar

S. No	Topics	No. of Periods	Book(s) followed	Topics for self Study
UNIT-I: CRYSTAL GROWTH, WAFER PREPARATION, EPITAXY AND OXIDATION				
1.	Clean room and safety requirements	1	R1	Wafer preparation for PMOS ,NMOS ,CMOS and Bi-CMOS device fabrication
2.	Electronic grade silicon – Basic steps in IC fabrication-crystal plane and orientation – Defects in the lattice	1	T1	
3.	Czochralski crystal growing silicon shaping	1	T1	
4.	Processing considerations	1	T1	
5.	Vapour phase epitaxy–Liquid phase epitaxy-selective epitaxy-	1	T1	
6.	Molecular beam epitaxy - Epitaxial Evaluation –	1	T1	
7.	Growth mechanism and kinetics	1	T1	
8.	Thin oxides	1	T1	
9.	Oxidation Techniques and systems – Oxide properties	1	T1	
10.	Redistribution of dopants at interface	1	T1	
11.	Oxidation of polysilicon	1	T1	
12.	Oxidation induced effects.	1	T1	
Total periods required:		**12**		
UNIT- II: LITHOGRAPHY AND RELATIVE PLASMA ETCHING				
13.	Mask Making	1	T1	Lithography for PMOS ,NMOS ,CMOS and Bi-CMOS device
14.	Optical lithography	1	T1	

15.	Electron lithography	1	T1	fabrication
16.	X-ray lithography	1	T1	
17.	Ion lithography	1	T1	
18.	Plasma properties	1	T1	
19.	Feature size control and Anisotropie Etch mechanism	2	T1	
20.	Feature size control and Anisotropie Etch mechanism	1	T1	
21.	Relative plasma etching Techniques and Equipments	1	T1	
Total periods required:		**10**		
UNIT-III : DEPOSITION, DIFFUSION , ION IMPLANTATION				
22.	Deposition process – polisilicon	2	T1	Diffusion Diffusion Ion implantation for PMOS ,NMOS ,CMOS and Bi-CMOS device fabrication
23.	plasma assisted deposition	1	T1	
24.	models of diffusion in solids	1	T1	
25.	Fick's one dimensional diffusion equation	1	T1	
26.	Atomic diffusion mechanism	1	T1	
27.	Measurement Techniques	1	T1	
28.	Range theory – Carrier recovery due to annealing	2	T1	
29.	Implantation equipment	1	T1	
30.	Annealing Shalloe junction – high energy implantation – Physical vapour deposition – patterning	2	T1	
Total periods required:		**12**		
UNIT-IV: METALLIZATION				
31.	Metallization applications – metallization choices	2	T1	Metallization for PMOS ,NMOS ,CMOS and Bi-CMOS device fabrication
32.	Metallization problems	2	T1	
33.	New role of metallization	1	T1	
34.	metallization systems	1	T1	

35.	sputtering – problems associated with Al – Cu interconnect	2	T1	
36.	Comparison of RC delay of Polysilicon, Al.	2	T1	
Total periods required:		**10**		
UNIT-V : ANALYTICAL, ASSEMBLY TECHNIQUES & PACKAGING OF VLSI DEVICES				
37.	Analytical beams – Beams specimen interaction	2	T1	**Research Topics:** sub-micron and nano fabrication processes
38.	Chemical methods	1	T1	
39.	package types	1	T1	
40.	packing design considerations	1	T1	
41.	VLSI assembly technology	2	T1	
42.	Package Fabrication Technology	2	T1	
Total periods required:		**09**		
Grand total periods required:		**53**		

TEXT BOOKS

T1: S.M.Sze "VLSI Technology", Tata Mcgraw Hill,2nd edition, 1988.

REFERENCES BOOKS

R1: Sorab. K. Gandhi "VLSI Fabrication and Principles", John wiley and sons, 1983.

R2: Amar Mukherjee "Introduction to NMOS & CMOS VLSI system Design", Prentice Hall, 1986.

R3: Mccanny and J.C.White "VLSI Technology and design", Academic Press, 1987.

R4: Dasgupta "VLSI Technology", Pearson Education Pvt Ltd 2001.

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Lesson Plan

Name of the Subject: LOW VOLTAGE ANALOG CIRCUIT DESIGN (14MT15708)
Class & Semester: M. Tech. (VLSI) – I Semester
Name of the faculty Member: K.NEELIMA

S. No.	Topic	No. of periods	Book(s) followed	Topics for self study
UNIT – I: INTRODUCTION TO LOW VOLTAGE DESIGN				
1.	Low-voltage analog circuit design challenges	1	R2	Low Power design Considerations.
2.	Design for Low power	2	T1	
3.	Low Power Circuit technologies	2	T1	
4.	Techniques for Leakage Power Reduction	2	T1	
5.	Dynamic Voltage Scaling	2	T1	
Total periods required:		**09**		
UNIT – II: FGMOS, CIRCUIT APPLICATIONS AND DESIGN TECHNIQUES				
6.	The FGMOS Device	1	R1	FGMOS based Applications.
7.	Designing with FGMOS	2	R1	
8.	Minimum Input Capacitance	2	R1	
9.	Initial Design ideas	2	R1	
10.	Circuit Applications and design Techniques	2	R1	
Total periods required:		**09**		
UNIT -III: DESIGN FOR LOW POWER				
11.	Lightweight Embedded Systems	3	T1	Power estimation of Various Circuits.
12.	Low-Power Design of Systems on Chip	3	T1	
13.	Implementation- Level Impact on Low Power Design	2	T1	
14.	Accurate Power estimation of combinational CMOS digital Circuits	2	T1	
15.	Clock Powered CMOS for Energy-Efficient Computing	2	T1	
Total periods required:		**12**		
UNIT -IV: Analog RF CMOS Circuits - I				
16.	Power Considerations – sources of power Dissipation	2	T2	Limitations in Design of Receivers.
17.	Limits in Power dissipation	2	T2	

18.	V_{DD} Downscaling	2	T2	
19.	Front-End Challenges	3	T2	
20.	Superheterodyne architecture	3	T2	
Total periods required:		**12**		
UNIT -V: Analog RF CMOS Circuits - II				
21.	Technology Structural Alternatives	2	T2	PLL Design Considerations. **Research Topics:** Low Voltage Analog HF Circuits.
22.	schematic Design Techniques for power saving in RF	2	T2	
23.	RF Amplifier Design	3	T2	
24.	Mixer Design	3	T2	
25.	PLL Design	3	T2	
Total periods required:		**13**		
Grand total periods required:		**55**		

TEXT BOOKS:

T1: Vojin G.Oklobdzija,"Digital Design and Fabrication", CRC Press, 2nd edition, 2008.

T2: Unai Alvarado, Guillermo Bistue and Inigo Adin, "Low Power RF Circuit Design in standard CMOS Technology", Springer, 2011.

REFERENCE BOOKS:

R1: Dr Esther Rodriguez-Villegas,"Low Power and Low Voltage Circuit Design with the FGMOS Transistor", The Institution of Engineering and Technology, 2006.

R2: Shouri Chatterjee, Kong Pang Pun, et al,"Analog Circuit Design Techniques at 0.5V",springer,2007.

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SREE VIDYANIKETHAN ENGINEERING COLLEGE
(Autonomous)
Sree Sainath Nagar, A. Rangampet-517 102

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Lesson Plan

Name of the Subject: Research Methodology (14MT10310)
Name of the faculty Member:
Class & Semester: M. Tech. - I Semester **Section:**

S. No.	Topic	No. of periods required	Book(s) followed	Topics for self study
Unit-I: Introduction to Research Methodology				
1.	Research objective and Motivation	1	T1	Problems encountered by researchers.
2.	Types of Research –Descriptive vs Analytical, Applied vs Fundamental, Quantitative vs Qualitative, Conceptual vs Empirical	1	T1	
3.	Research Approaches	1	T1	
4.	Research and Scientific Methods	1	T1	
5.	Research Process	2	T1	
6.	Criteria of Good Research	1	T1	
	Total of periods required:	**7**		
Unit-II: Research Problem and Design				
7.	What is Research Problem?	1	T1	Experimental designs. Developing research plan.
8.	Selecting the Problem	1	T1	
9.	Necessity of Defining the Problem	1	T1	
10.	Techniques involved in Defining a Problem	2	T1	
11.	What is Research Design? Its need and features	1	T1	
12.	Important concepts of Research Design	1	T1	
13.	Designing Methods: Research design in case of exploratory research studies, Research design in case of descriptive and diagnostic research studies, Research design in case of hypothesis-testing research studies	2	T1	
	Total of periods required:	**9**		
Unit-III: Data Collection, Analysis, and Hypothesis				
14.	Collection of Primary Data: Observation Method, Interview Method, Questionnaires, Schedules, Other Methods	1	T1	Guidelines for constructing questionnaires and interviews.
15.	Collection of Secondary Data	1	T1	
16.	Selection of Appropriate Method for Data Collection	1	T1	
17.	Processing Operations: Editing, Coding, Classification and Tabulation	2	T1	
18.	Types of Analysis	1	T1	
19.	What is Hypothesis? Basic Concepts of Testing Hypothesis: Null hypothesis and alternative hypothesis, Level of significance,	2	T1	

	Decision rule, Type I and Type II errors, Two-tailed and One-tailed tests			
20.	Hypothesis Testing Procedure	1	T1	
	Total of periods required:	**9**		
Unit-IV: Statistics in Research				
21.	Review of Statistical Techniques: Mean, Median, Mode	1	T1	Simple regression analysis.
22.	Geometric Mean, Harmonic Mean, Variance, Standard Deviation	1	T1	
23.	Measure of Asymmetry	1	T1	
24.	Normal Distribution	2		
25.	Chi-Square as a Test for Comparing Variance	1	T1	
26.	Steps Involved in Applying Chi-Square Test	1	T1	
27.	Problems	2		
	Total of periods required:	**9**		
Unit-V: Interpretation and Report Writing				
28.	Interpretation: Meaning, Importance	1	T1	Mechanics of writing research report.
29.	Interpretation: Techniques and Precautions	1	T1	
30.	Report Writing: Significance and Different Steps	2	T1	
31.	Types of Reports	1	T1	
32.	Precautions in Report Writing	1	T1	
	Total of periods required:	**6**		
	Grand total of periods required:	**40**		

Text Book:

T1. C.R. Kothari, *Research Methodology: Methods and Techniques*, New Age International Publishers, New Delhi, 2nd Revised Edition, 2004.

Reference Books:

R1. Ranjit Kumar, *Research Methodology: A step-by-step guide for beginners*, Sage South Asia, 3rd ed., 2011.

R2. R. Panneerselvam, Research Methodology, PHI learning Pvt. Ltd., 2009

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SREE VIDYANIKETHAN ENGINEERING COLLEGE
(Autonomous)
Sree Sainath Nagar, A. Rangampet-517 102

Department of Electronics and communication Engineering

Lesson Plan

Name of the Subject: ULSI Technology (14MT15709)
Class & Semester: M. Tech. (VLSI) – I Semester
Name of the faculty Member:

S. No.	Topic	No. of periods	Book(s) followed	Topics for self study
	UNIT – I			
1.	**Cleanroom technology**- Intoduction, cleanroom classification	1	T1	Transmission Electron Microscopy (TEM)
2.	cleanroom design concept	1	T1	
3.	cleanroom installation	1	T1	
4.	cleanroom operation	1	T1	
5.	Automation, related facility systems	1	T1	
6.	**Wafer-cleaning technology**- Introduction, basic concepts of wafer cleaning	1	T1	
7.	Wet-cleaning technology	1	T1	
8.	Dry-cleaning technology	1	T1	
9.	ULSI Process Technology	2	T2	
	Total periods required:	**10**		
	UNIT – II			
10.	**Epitaxy**- Introduction, Fundamental Aspects of Epitaxy	1	T1	
11.	Conventional Si Epitaxy	1	T1	
12.	Low temperature Epitaxy of Si	1	T1	
13.	Selective Epitaxial Growth of Si	1	T1	
14.	Characterization of Epitaxial films	1	T1	
15.	**Conventional and Rapid Thermal Processes**- Introduction, Requirements for Thermal Processes	1	T1	
16.	Rapid Thermal Processing	1	T1	
17.	**Dielectric and Polysilicon Film Deposition**- Introduction, Deposition Processes	1	T1	
18.	APCVD Silicon Oxides	1	T1	
19.	LPCVD Silicon Oxides	1	T1	
20.	LPCVD Silicon Nitrides	1	T1	
21.	LPCVD Polysilicon Films	1	T1	
22.	Plasma Assisted Depositions	1	T1	
23.	Other Deposition Methods	1	T1	
24.	Applications of Deposited Polysilicon, Silicon Oxide and Silicon Nitride Films.	1	T1	
	Total periods required:	**16**		

		UNIT -III		
25.	**Lithography**- Introduction, Optical Lithography	1	T1	Interconnects
26.	Electron Lithography	1	T1	
27.	X-Ray Lithography	1	T1	
28.	Ion Lithography	1	T1	
29.	**Etching**- Introduction, Low-Pressure Gas Discharge	1	T1	
30.	Etch Mechanisms	1	T1	
31.	Reactive Plasma Etching Techniques and Equipment	1	T1	
32.	Plasma Processing Processes	1	T1	
33.	Diagnostics, End Point Control and Damage	1	T1	
34.	Wet Chemical Etching	1	T1	
35.	**Metallization**- Metal Deposition Techniques	1	T1	
36.	Silicide Process	1	T1	
37.	CVD Tungsten Plug and Other Plug Processes	1	T1	
38.	Multilevel Metallization	1	T1	
39.	Metallization Reliability	1	T1	
	Total periods required:	**15**		
		UNIT – IV		
40.	**Process integration**- Introduction, Basic Process Modules and Device Considerations for ULSI	1	T1	
41.	CMOS Technology	1	T1	
42.	Bipolar Technology	1	T1	
43.	BiCMOS Technology	1	T1	
44.	MOS Memory Technology	1	T1	
45.	Process Integration Considerations in ULSI Fabrication Technology	1	T1	
	Total periods required:	**06**		
		UNIT – V		
46.	**Assembly and Packaging**-Introduction, package types,	1	T1	Relations between DC and AC Lifetimes, Some Recent ULSI Reliability Concerns, Mathematics of Failure Distribution. ULSI devices: DRAM cell, SRAM cell. **Research Topics:** Advance Interconnects
47.	ULSI Assembly Technologies, Package Fabrication Technologies	1	T1	
48.	Package Design Considerations,	1	T1	
49.	Special Package Considerations, Other ULSI Packages.			
50.	**Reliability**- Introduction, Hot Carrier Injection	1	T1	
51.	Electromigration,	1	T1	
52.	Stress Migration	1	T1	
53.	Oxide Breakdown, Effect of Scaling on Device Reliability	1	T1	
	Total periods required:	**07**		

Grand total periods required:	58

Text Books:

T1. C.Y.Chang, S.M.Sze,ULSI Technology, McGraw-Hill,2000.

T2. Chih-Hang Tung, George T.T.Sheng, Chih-Yuan Lu, ULSI Semiconductor Process Technology Atlas, John Wiley & Sons, 2003.

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