

SREE VIDYANIKETHAN ENGINEERING COLLEGE (AUTONOMOUS)
SREE SAINATH NAGAR, A. RANGAMPET-517 102



Department of Computer Science and Engineering
LESSON PLAN

Name of the Subject: DIGITAL LOGIC DESIGN

Name of the faculty Member: Mr. D.R. Kumar Raja

Class & Semester: II B. Tech I Semester

Section: CSSE-B

S. No.	Topic	No. of periods	Book(s) followed	Topics for self study
UNIT-I: BINARY SYSTEMS				
1	Digital Systems, Binary Numbers	1	T1	Binary Codes, Digital Logic Families
2	Number base conversions	1	T1	
3	Octal and Hexadecimal Numbers	1	T1	
4	Tutorial-1	1		
5	Complements	1	T1	
6	Signed binary numbers	1	T1	
7	Boolean Algebra, Boolean functions	1	T1	
8	Tutorial-2	1		
9	Canonical and standard forms	1	T1	
10	Other logic operations	1	T1	
11	Digital logic gates, Formative Test	1	T1	
12	Tutorial-3	1		
Total periods required:		12		
UNIT - II: GATE LEVEL MINIMIZATION				
13	The k-map method	1	T1	Prime Implicants - Method for Simplification of Boolean Functions
14	Four-variable map	1	T1	
15	Five-Variable map	1	T1	
16	Tutorial-4	1		
17	Product of sums simplification	1	T1	
18	Don't-care conditions	1	T1	
19	NAND and NOR implementation	1	T1	
20	Tutorial-5	1		
21	Other Two-level implementations	1	T1	
22	Exclusive - OR function, Formative Test	1	T1	
Total periods required:		10		
UNIT -III: COMBINATIONAL LOGIC				
23	Combinational Circuits	1	T1	Binary Multiplier Circuits
24	Tutorial-6	1		
25	Analysis procedure	1	T1	
26	Design Procedure	1	T1	
27	Binary Adder-Subtractor	1	T1	
28	Tutorial-7	1		
29	BCD Adder	1	T1	
30	Magnitude Comparator	1	T1	
31	Decoders	1	T1	
32	Tutorial-8	1		
33	Encoders	1	T1	

34	Multiplexers, De-Multiplexers, Formative test	1	T1	
Total periods required:		12		
UNIT – IV: SEQUENTIAL LOGIC				
35	Latches	1	T1	State Reduction and Assignment
36	Tutorial-9	1		
37	Flip-Flops	1	T1	
38	Analysis of clocked sequential circuits	1	T1	
39	Design of synchronous sequential	1	T1	
40	Tutorial-10	1		
41	Registers, shift registers	1	T1	
42	Ripple counters	1	T1	
43	Synchronous counters-1	1	T1	
44	Tutorial-11	1		
45	Synchronous counters-2	1	T1	
46	Ring Counter and Johnson Counter, Formative Test	1	T1	
Total periods required:		12		
UNIT – V: MEMORY AND PROGRAMMABLE LOGIC				
47	Random-Access Memory	1	T1	Asynchronous sequential circuits
48	Tutorial-12	1		
49	Memory Decoding	1	T1	
50	Error Detection and Correction	1	T1	
51	Read-only memory-1	1	T1	
52	Tutorial-13	1		
53	Read-only memory-2	1	T1	
54	Programmable logic Array	1	T1	
55	programmable Array logic	1	T1	
56	Tutorial-14	1		
57	Sequential Programmable Devices, Formative Test	1	T1	
Total periods required:		11		
Grand total periods required:		57		

TEXT BOOK:

T1. M. Morris Mano, "*Digital Design*", 3rded, Pearson Education/PHI, 1999

REFERENCE BOOKS:

R1. David J Comer, "*Digital Logic and State Machine Design*", Third Edition, Oxford University Press, 2012

R2. Charles H. Roth Jr, "*Fundamentals of Logic Design*", Fifth edition, Cengage Learning, 2008.

**Signature of the Faculty
Member**

**Signature of the Course
Coordinator**

Signature of the HOD

